

# CS16 T14 Logic Schematics

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73.BATTERY CHARGER(BQ24780S)

74.CHARGER SELECTOR

75.DC/DC VCC5M/VCC3M (TPS51285B)

76.DC/DC IMVP8 CONTROLLER(NCP81208)

77.DC/DC VCCCPUCORE(NCP81382)

78.DC/DC VCCGFXCORE\_I(NCP81382)

79.DC/DC VCCSA(NCP81382)

80.BLANK

81.BLANK

82.DC/DC VCC1R0\_SUS(BD91364BMUU)

83.LOAD SW VCCST & VCCSTG

84.DC/DC VCC1R2A(SN1409027)

85.DC/DC VCC0R6B(TPS51206)

86.DC/DC VCC2R5A(TLV62080)

87.DC/DC VCC1R8\_SUS(BU90104GWZ)

88.DC/DC VCCPCHCORE(NB682)

89.BLANK

90.BLANK

91.DC/DC VCCGFXCORE\_D (NCP81172)

92.DC/DC VCC1R35VIDEO (SN1409027)

93.LOAD SW PCH SUS

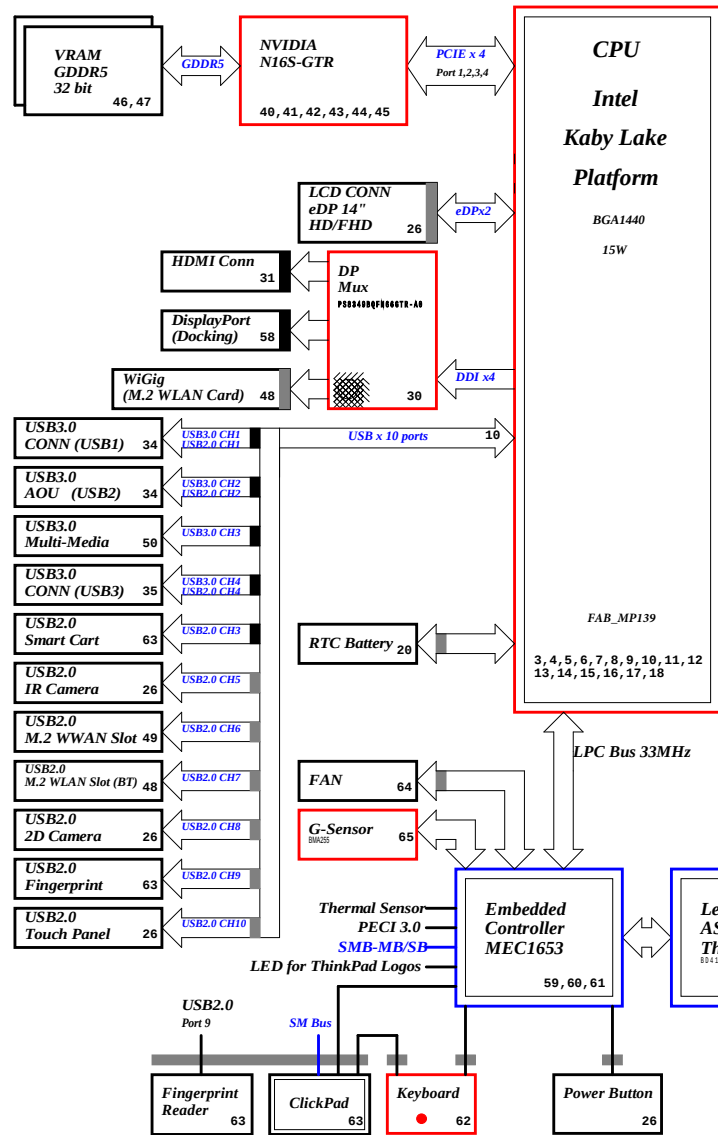
94.LOAD SW LAN

95.LOAD SW VIDEO

96.LOAD SW B

97.LOAD SW WWAN & WLAN

98.PTH FOR SCREW HOLES



# Windu Block Diagram

Project Code: CT470

2015 Dec ' 16

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC -55 to 125degC	+/-30ppm/degC +/-30ppm/degC	NPO C0G
-55 to 125degC -55 to 105degC -55 to 85degC	+/-15% +/-22% +/-15%	X7R X6S X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.25pF +/-0.5pF	C D
+/-5% +/-10% +/-20% +80/-20%	J K M Z

TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1810
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

↑  
LOGIC

## EC SMBus0 address

Device	Address
G-Sensor (KX023)	0011 110Xb

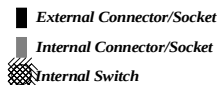
## PCH SM Bus address

Device	Address
CH-A DDR DIMM0 (J53)	1001 0000b
CH-B DDR DIMM1 (J43)	1001 0001b

FAB\_MP139

## PCH SM Bus0 address

Device	Address
Intel Lan_i219	0XC8



Security Classification	LC Future Center Secret Data	
Issued Date	2015/11/02	Deciphered Date
		2015/8/10
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Title		BLOCK DIAGRAM	
Size	Document Number	Rev	0.1
C			
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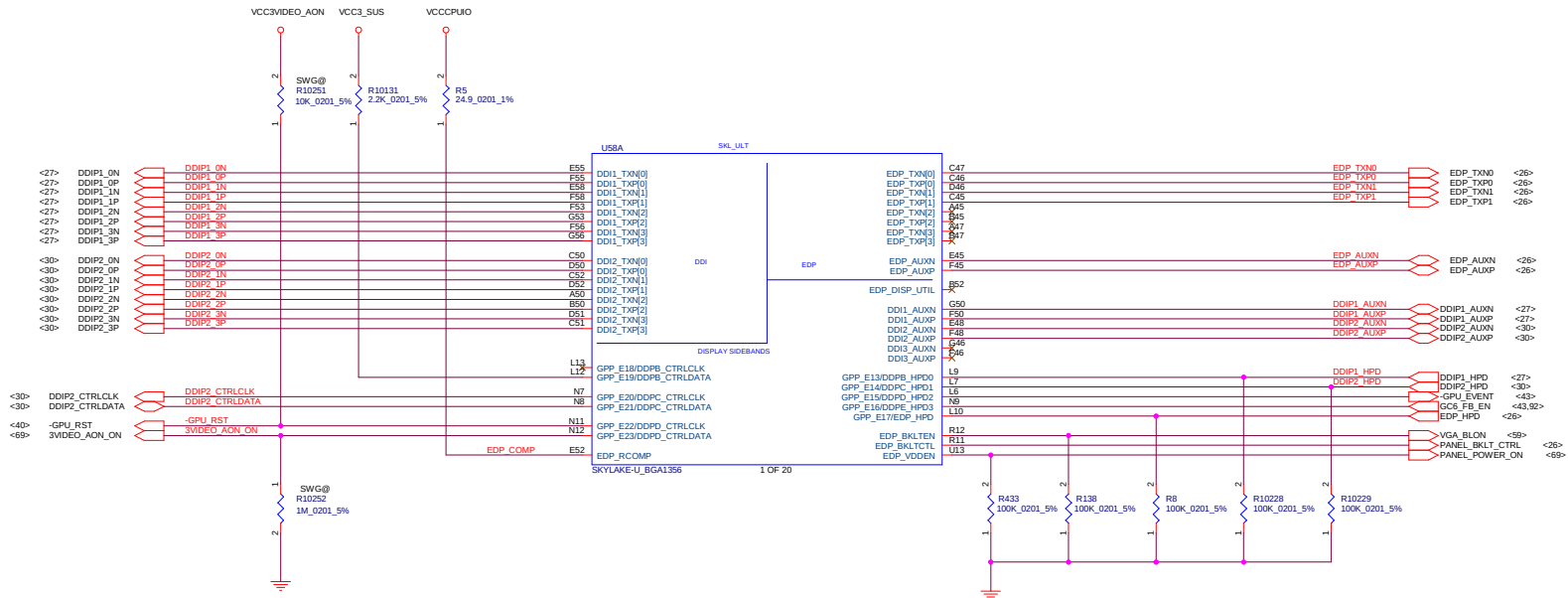


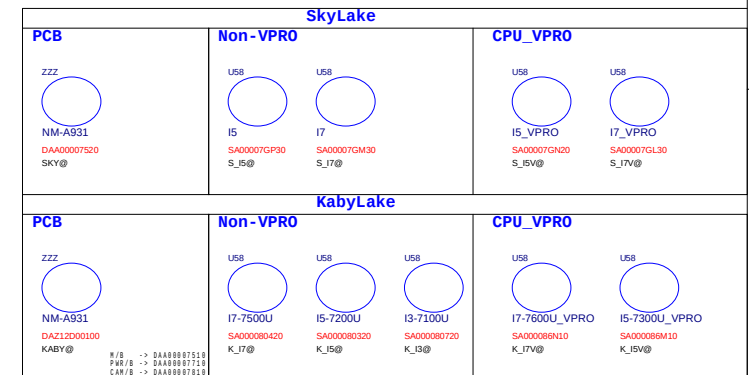
TABLE : Functional Strap

DDPB\_CTRLDATA

HIGH	Port B is detected.
LOW	Port B is not detected.

DDPC\_CTRLDATA

HIGH	Port C is detected.
LOW	Port C is not detected.



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Issued Date	2015/11/02	Deciphered Date	2015/8/10	Document Number	Rev
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	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
AU70	DDR0_DQ[14]	DDR0_DQ[14]	
AU69	DDR0_DQ[15]	DDR0_DQ[15]	
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
BA59	DDR0_DQ[30]	DDR0_DQ[46]	
AY59	DDR0_DQ[31]	DDR0_DQ[47]	
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BB37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
BA33	DDR0_DQ[46]	DDR1_DQ[14]	
BB33	DDR0_DQ[47]	DDR1_DQ[15]	
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
BA25	DDR0_DQ[62]	DDR1_DQ[46]	
BB25	DDR0_DQ[63]	DDR1_DQ[47]	

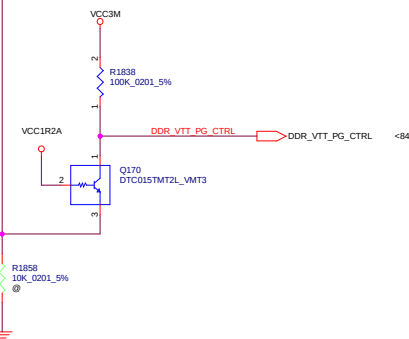
SKYLAKE-U BGA1356

	Pin	Interleave	Non-Interleave
Block 0	AM70 AM69 AT69 AT70	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]
Block 2	BA64 AY64 AY60 BA60	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]
Block 4	BA38 AY38 AY34 BA34	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]
Block 6	BA30 AY30 AY26 BA26	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]




Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

100%



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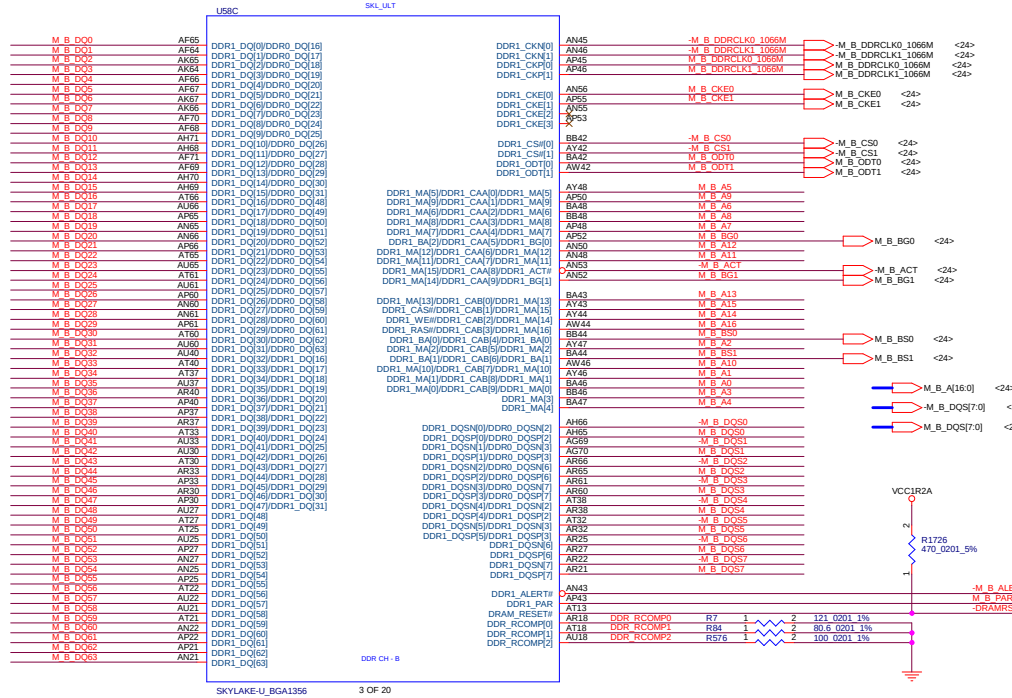
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TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC

<24> M\_B\_DQ[63:0]



TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_BA[2]	DDR1_CAB[5]	DDR1_BA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

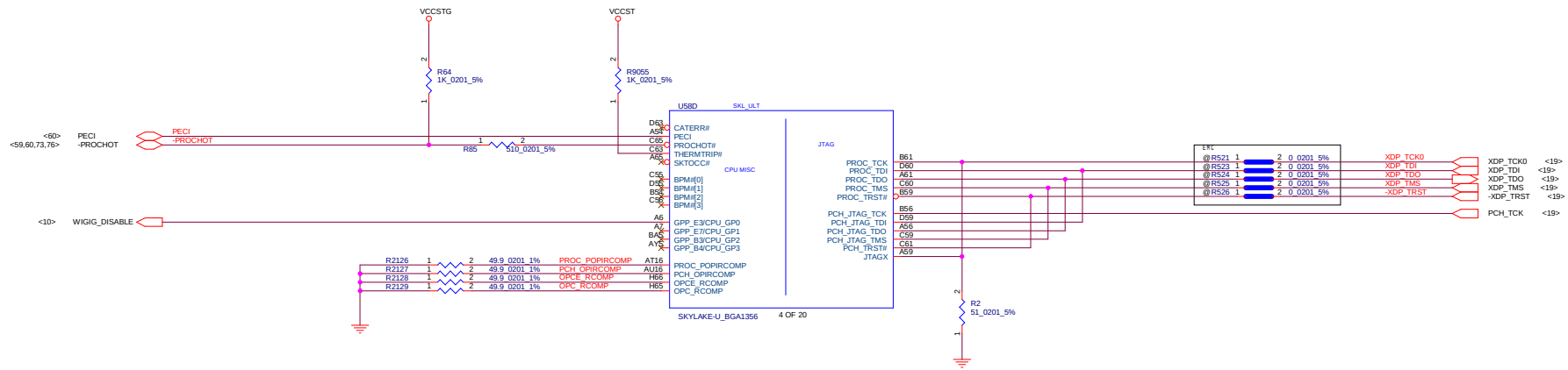


TABLE : Functional Strap

SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Functional Strap

SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

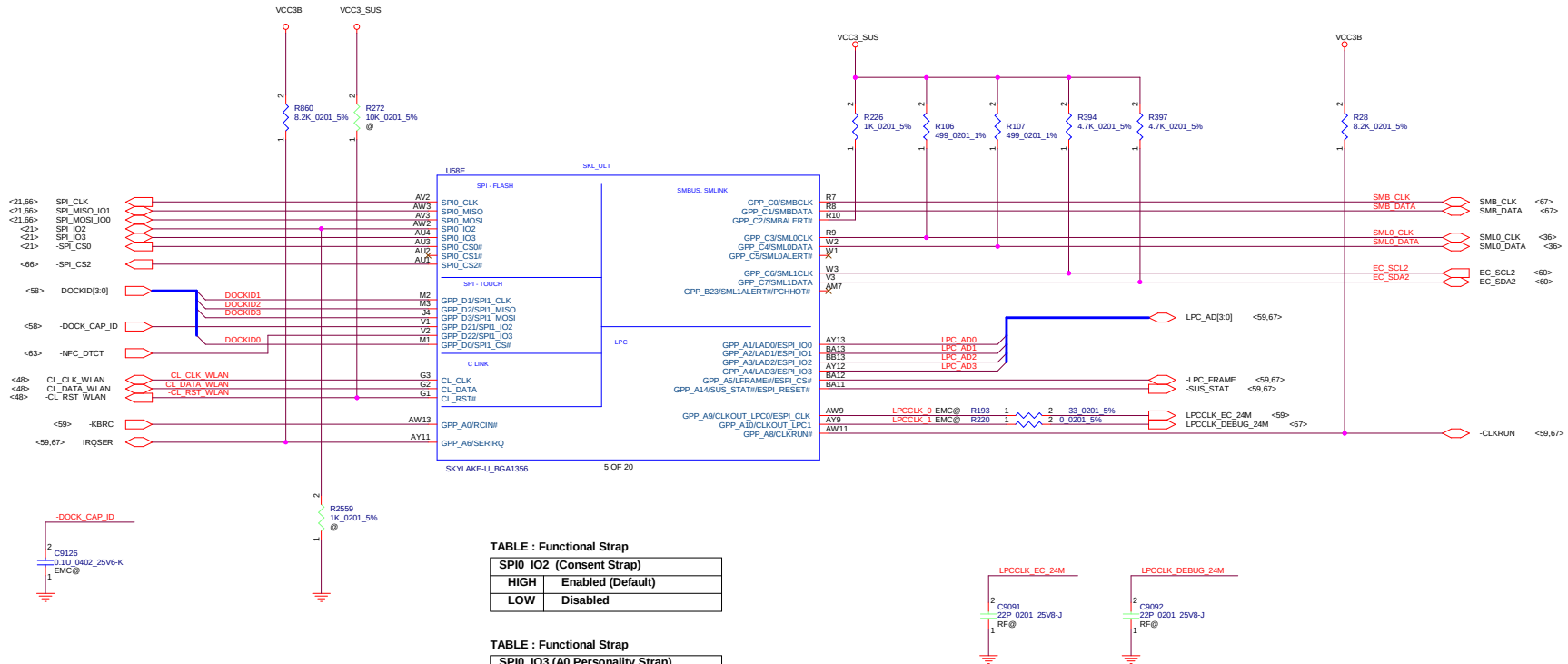


TABLE : Functional Strap

SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled



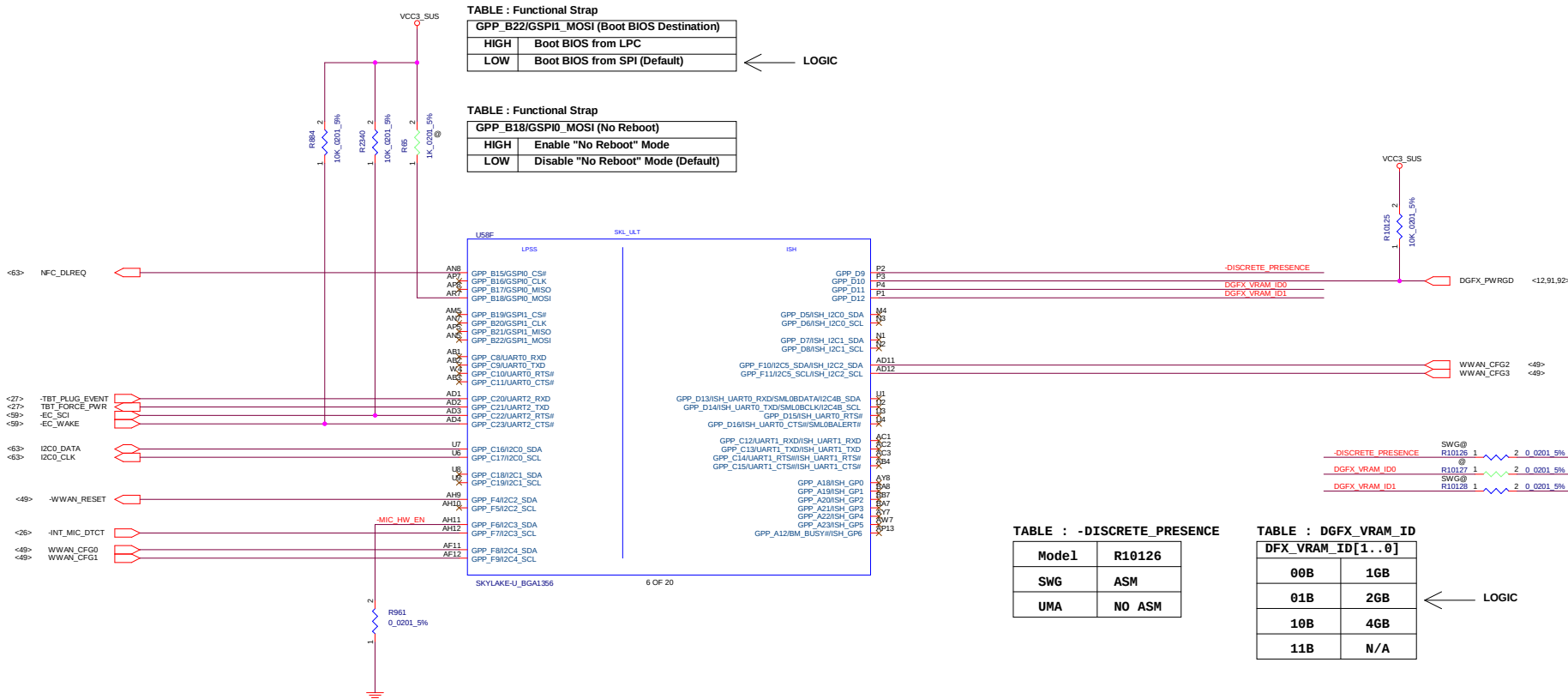


TABLE : Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

← LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

TABLE : -DISCRETE\_PRESENCE

Mode1	R10126
SWG	ASM
UMA	NO ASM

TABLE : DGFX\_VRAM\_ID

DFX_VRAM_ID[1..0]	
00B	16B
01B	26B
10B	46B
11B	N/A

← LOGIC



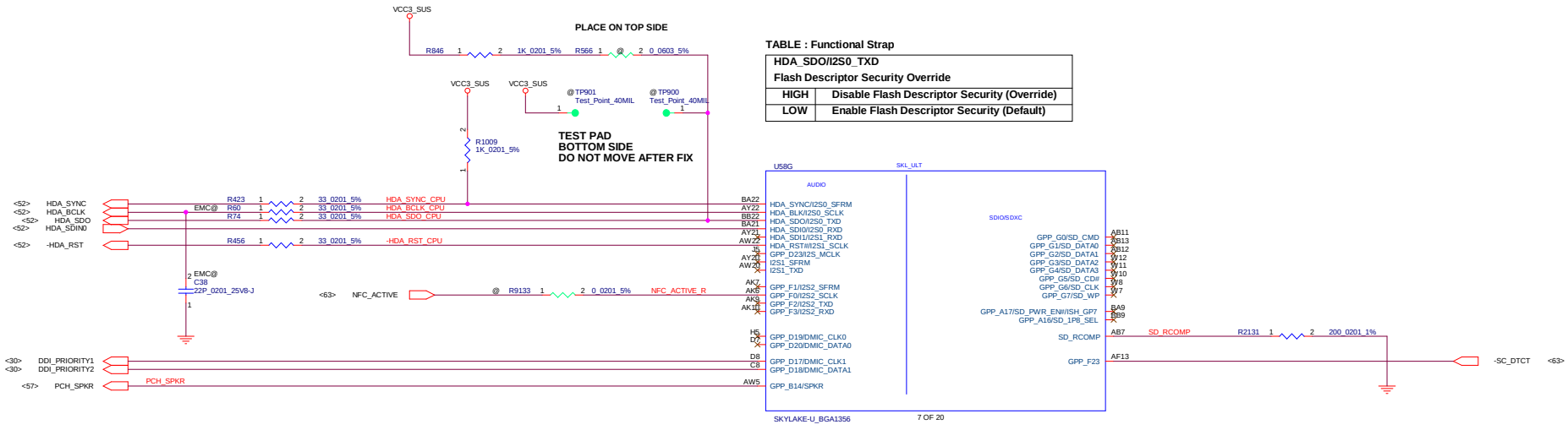


TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

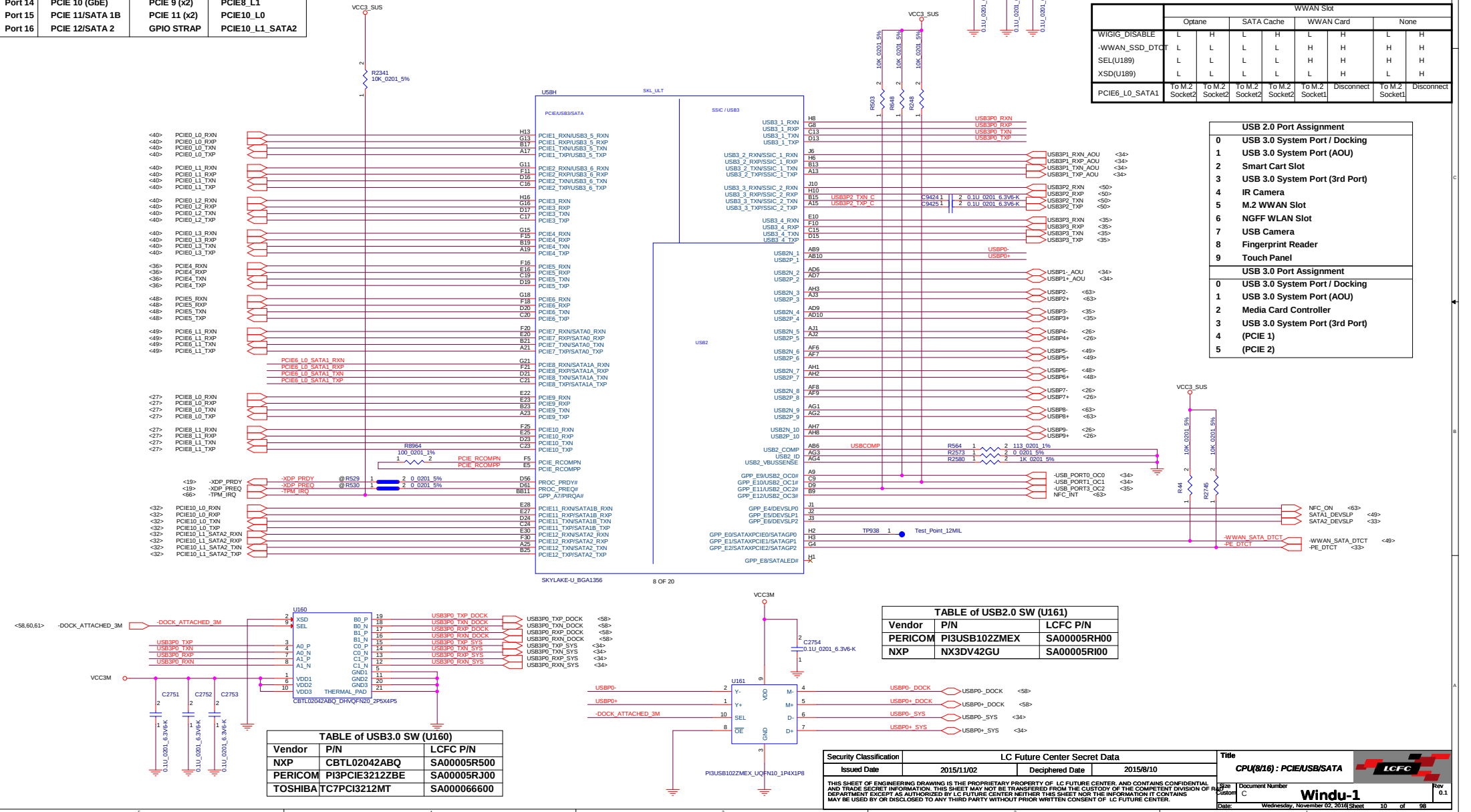
← LOGIC

Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	USB3 2	USB3P1
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1 (x4)	PCIE0
Port 6	USB3 6/PCIE 2	PCIE 2 (x4)	PCIE0
Port 7	PCIE 3 (GbE)	PCIE 3 (x4)	PCIE0
Port 8	PCIE 4 (GbE)	PCIE 4 (x4)	PCIE0
Port 9	PCIE 5 (GbE)	PCIE 5 (GbE)	PCIE4
Port 10	PCIE 6	PCIE 6	PCIE5
Port 11	PCIE 7/SATA 0	PCIE 7 (x2)	PCIE6_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE6_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x2)	PCIE8_L0
Port 14	PCIE 10 (GbE)	PCIE 9 (x2)	PCIE8_L1
Port 15	PCIE 11/SATA 1B	PCIE 11 (x2)	PCIE10_L0
Port 16	PCIE 12/SATA 2	GPIO STRAP	PCIE10_L1_SATA2

PCIe Port Assignment	
0 (x4)	Discrete GPU
4	GbE PHY
5	M.2 WLAN Slot Port 0
6 (x2)	Optane x2 or M.2 WLAN Slot Port 1x1
8 (x2)	Alpine Ridge-LP
10 (x2)	Main Storage x 2

SATA Port Assignment	
0 (PCIE 7)	
1A	SATA SSD on WWAN slot
1B (PCIE 11)	
2	SATA SSD Main Storage

TABLE of USB3.0 SW (U189)		
Vendor	P/N	LCFC P/N
NXP	CBTL02042ABQ	SA00005R500
PERICOM	PI3PCIE3212ZBE	SA00005R300
TOSHIBA	TC7PCI3212MT	SA000066600



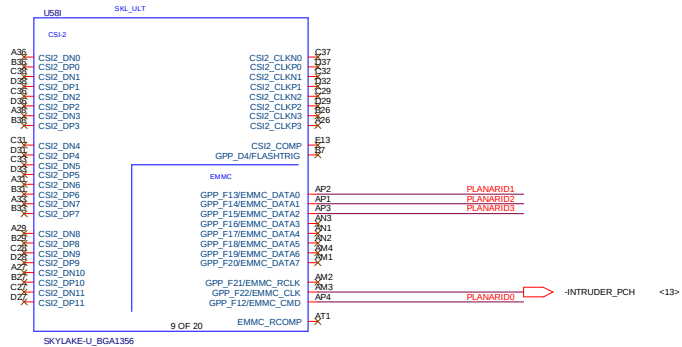
	WWAN Slot						
	Optane		SATA Cache		WWAN Card	None	
WIGIG_DISABLE	L	H	L	H	L	H	L
-WWAN_SSD_DTCT	L	L	L	L	L	H	H
SEL(U189)	L	L	L	L	H	H	H
XSD(U189)	L	L	L	L	L	H	L
PCIE6_L0_SATA1	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	To M.2 Socket1	Disconnect	To M.2 Socket1

USB 2.0 Port Assignment	
0	USB 3.0 System Port / Docking
1	USB 3.0 System Port (AOU)
2	Smart Card Slot
3	USB 3.0 System Port (3rd Port)
4	IR Camera
5	M.2 WWAN Slot
6	NGFF WLAN Slot
7	USB Camera
8	Fingerprint Reader
9	Touch Panel
USB 3.0 Port Assignment	
0	USB 3.0 System Port / Docking
1	USB 3.0 System Port (AOU)
2	Media Card Controller
3	USB 3.0 System Port (3rd Port)
4	(PCIE 1)
5	(PCIE 2)

TABLE of USB3.0 SW (U160)		
Vendor	P/N	LCFC P/N
NXP	CBTL02042ABQ	SA00005R500
PERICOM	PI3PCIE3212ZBE	SA00005R300
TOSHIBA	TC7PCI3212MT	SA000066600

TABLE of USB2.0 SW (U161)		
Vendor	P/N	LCFC P/N
PERICOM	PI3USB102ZMEX	SA00005RH00
NXP	NX3DV42GU	SA00005RI00

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Doc Number	C	Rev	0.1	Windu-1		
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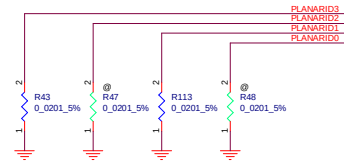


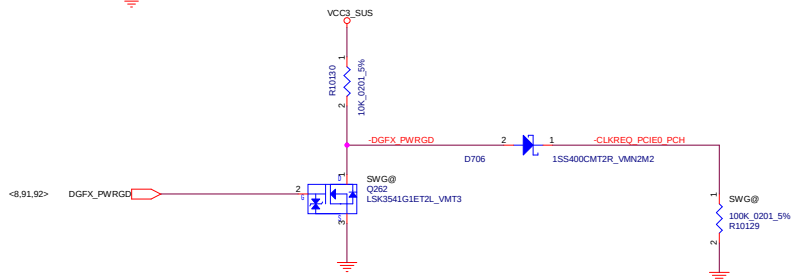
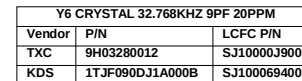
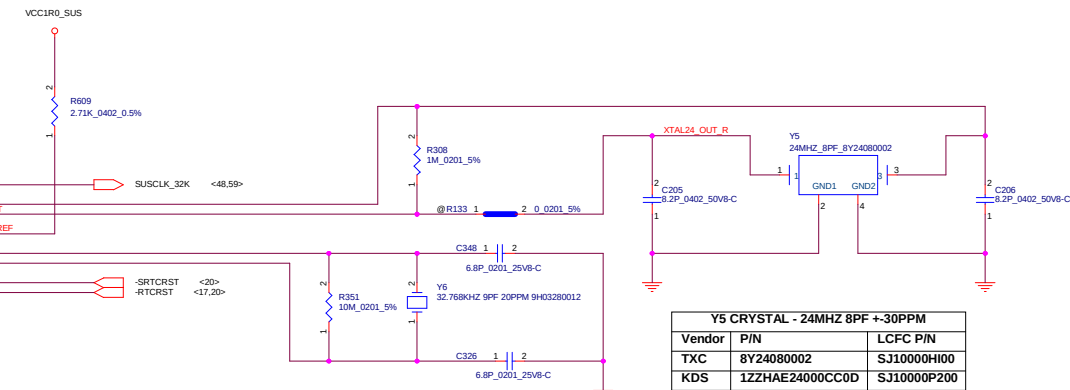
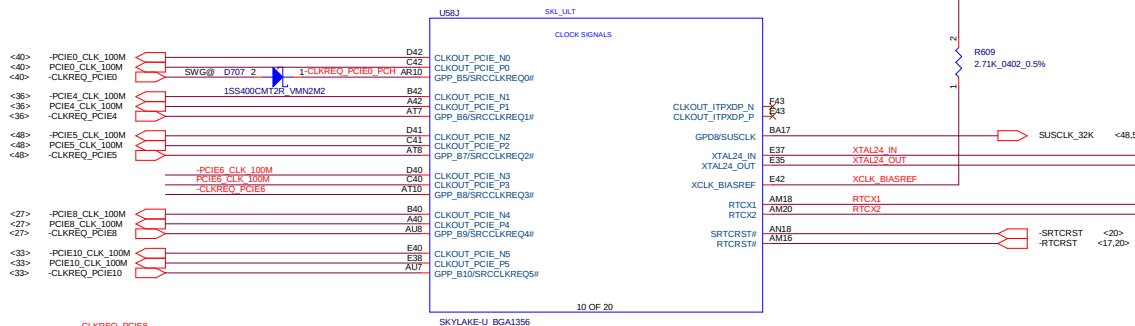
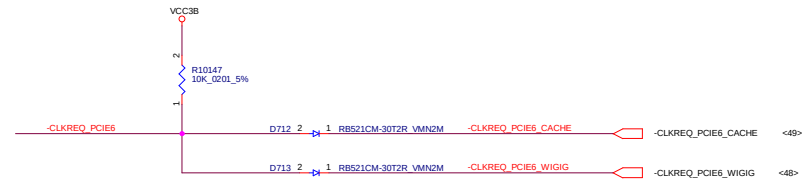
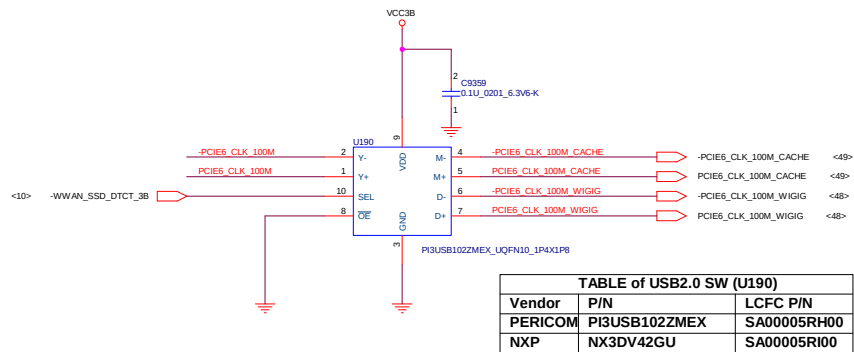
TABLE

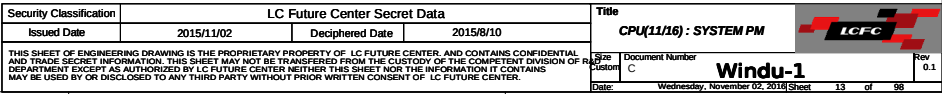
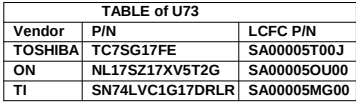
LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

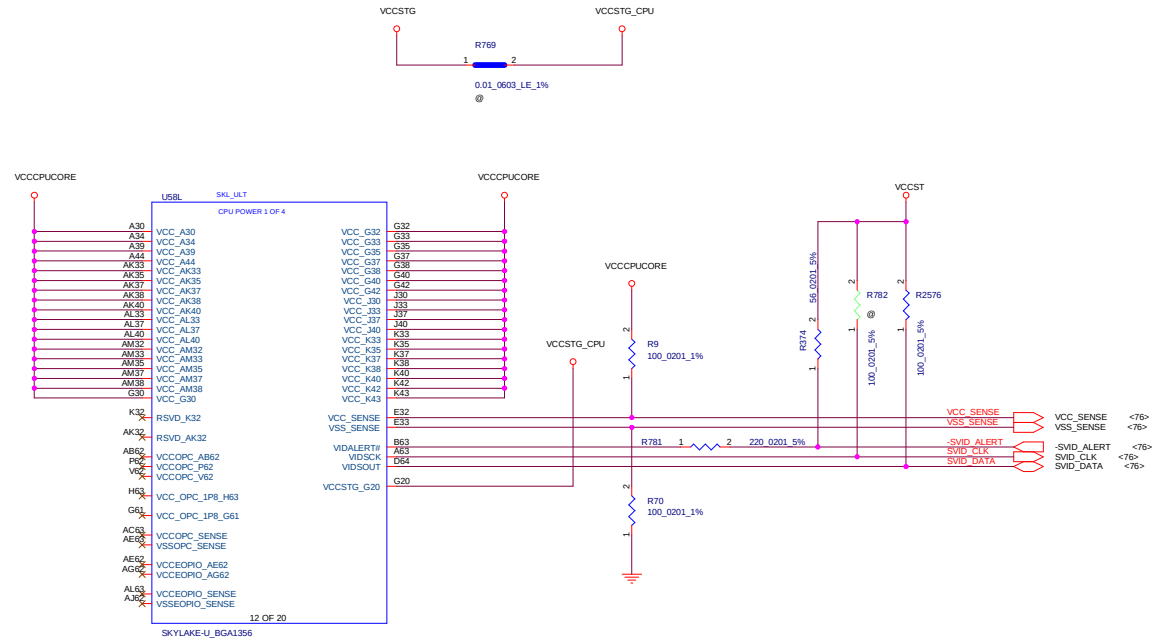
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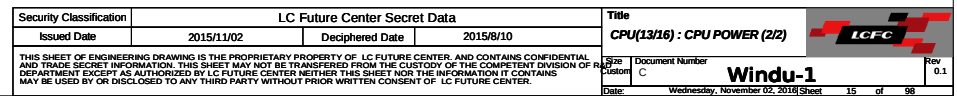
LEVEL	PLANARID[3..0]
SDV	0000B
FVT	0001B
FVT-2	0010B
SIT	0011B
SIT-R	0100B
SVT	0101B



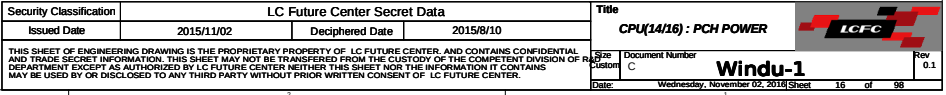




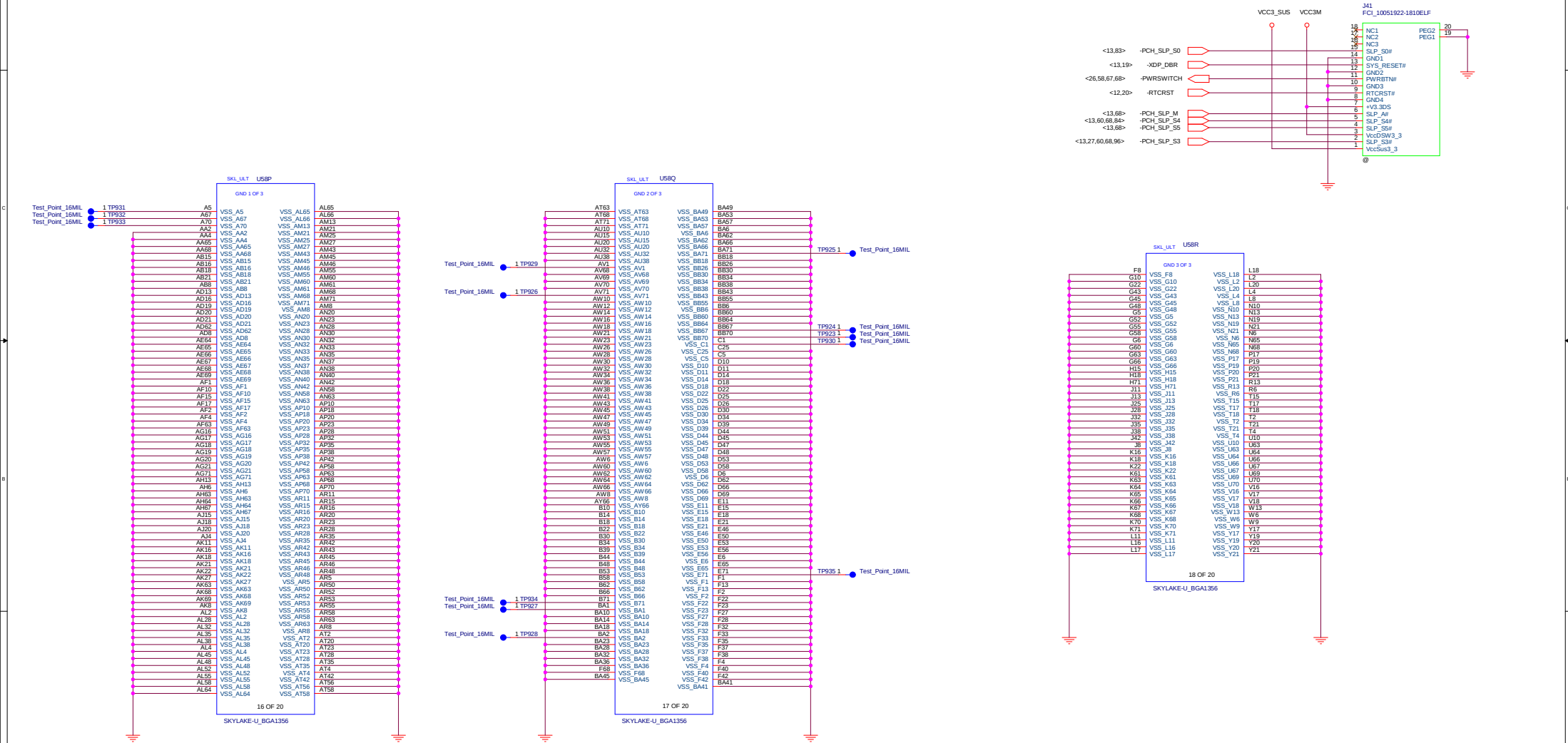






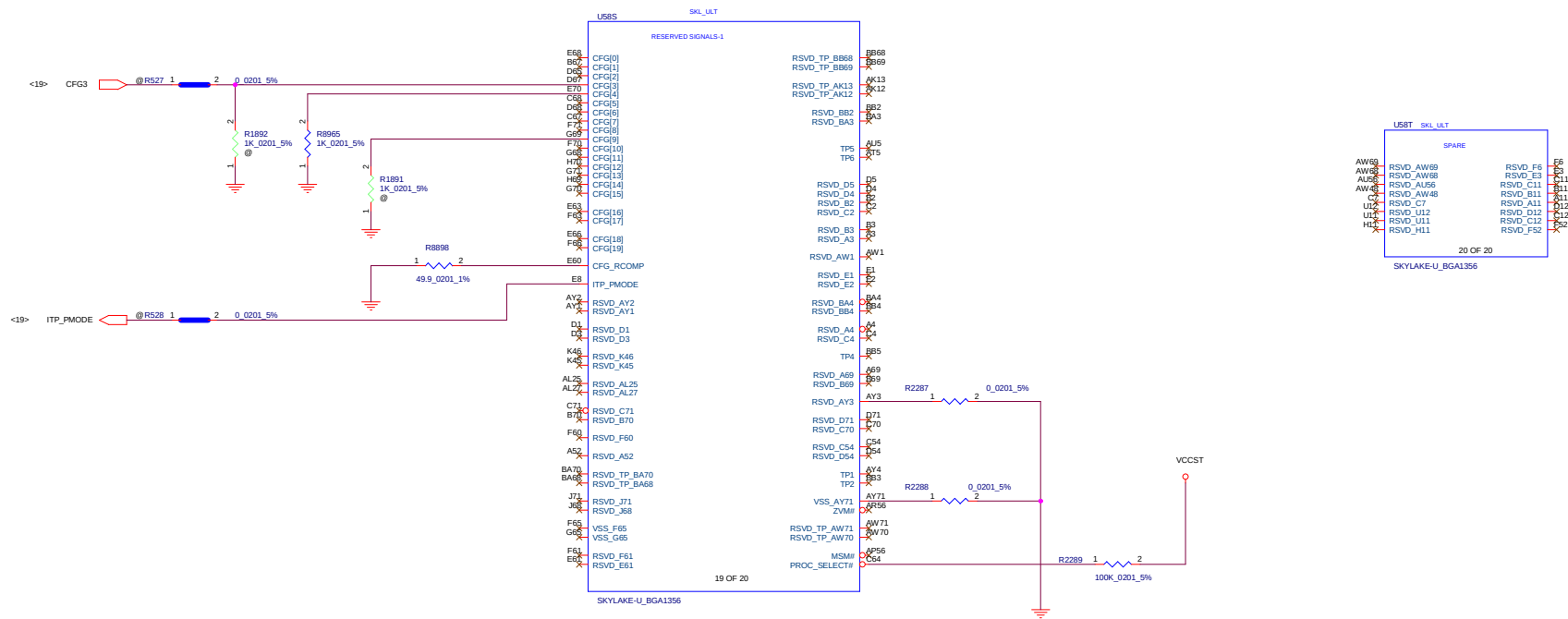


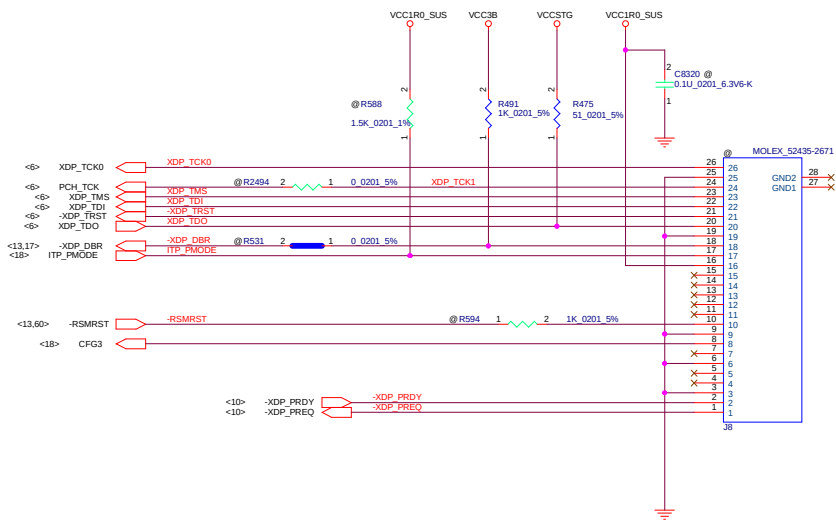
# APS/PETS Interface



TABLE

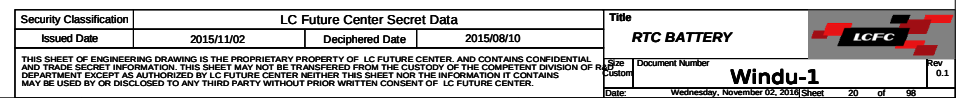
CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] setting 0 : MSR (C80h) bit[0] overridden
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled





TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 6	R2	ASM	ASM
Page 7	R2559	ASM	NO_ASM
Page 18	R1892	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	R588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM



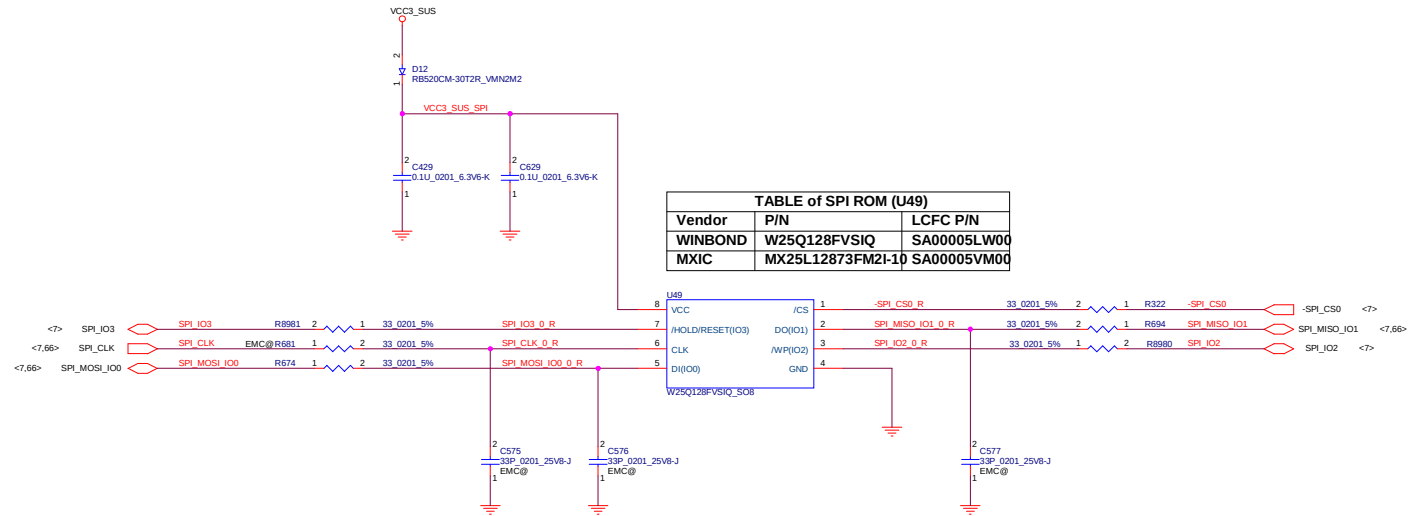
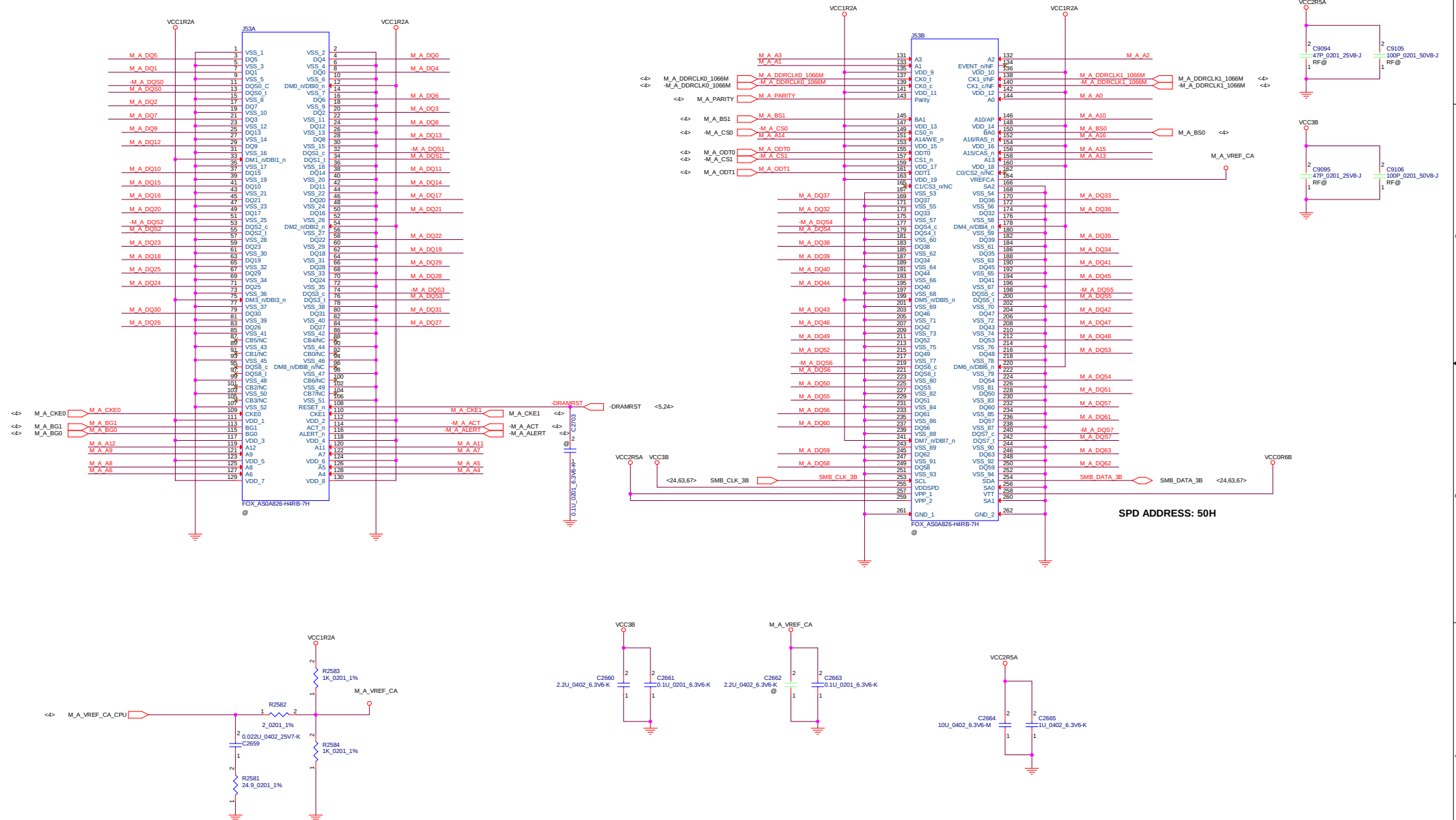


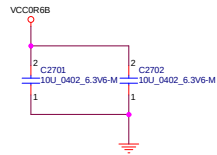
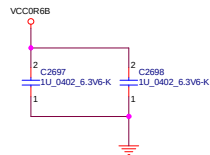
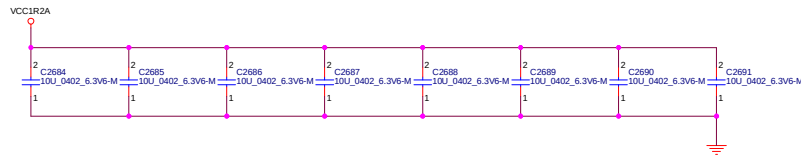
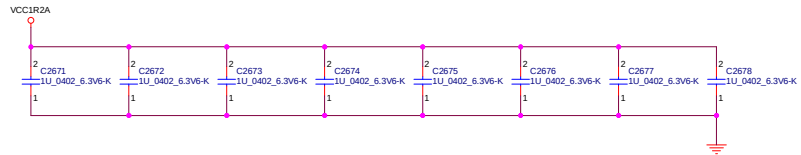
TABLE of SPI ROM (U49)		
Vendor	P/N	LCFC P/N
WINBOND	W25Q128FVSIQ	SA00005LW00
MXIC	MX25L12873FM21-10	SA00005VM00

TABLE							
SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	R861.2	CLK	4		
5	MISO	R694.2	R674.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

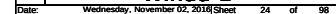
<4> M\_A\_DQ[63:0]  
<4> -M\_A\_DQS[7:0]  
<4> M\_A\_DQS[7:0]  
<4> M\_A\_A[16:0]

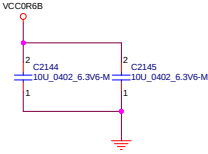
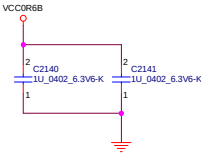
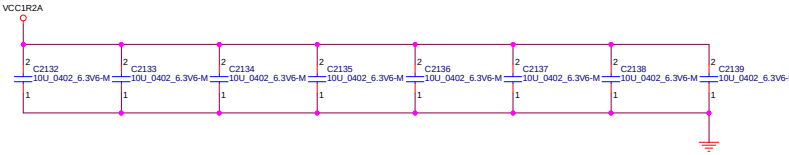
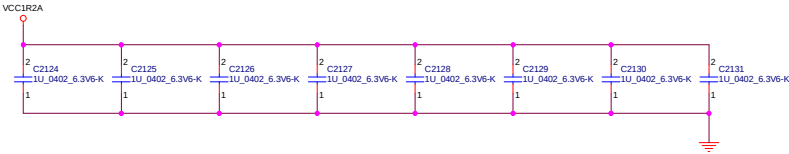






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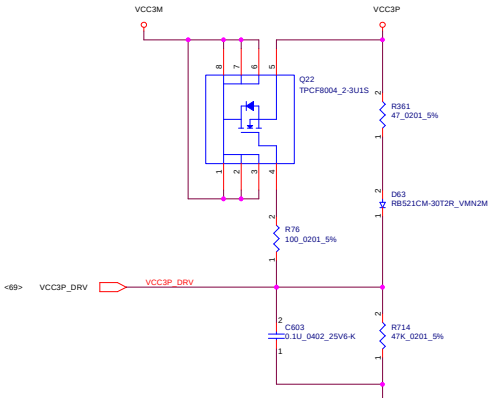




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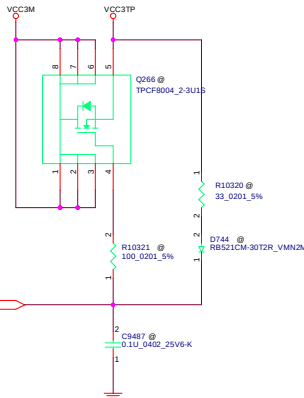


Windu-1

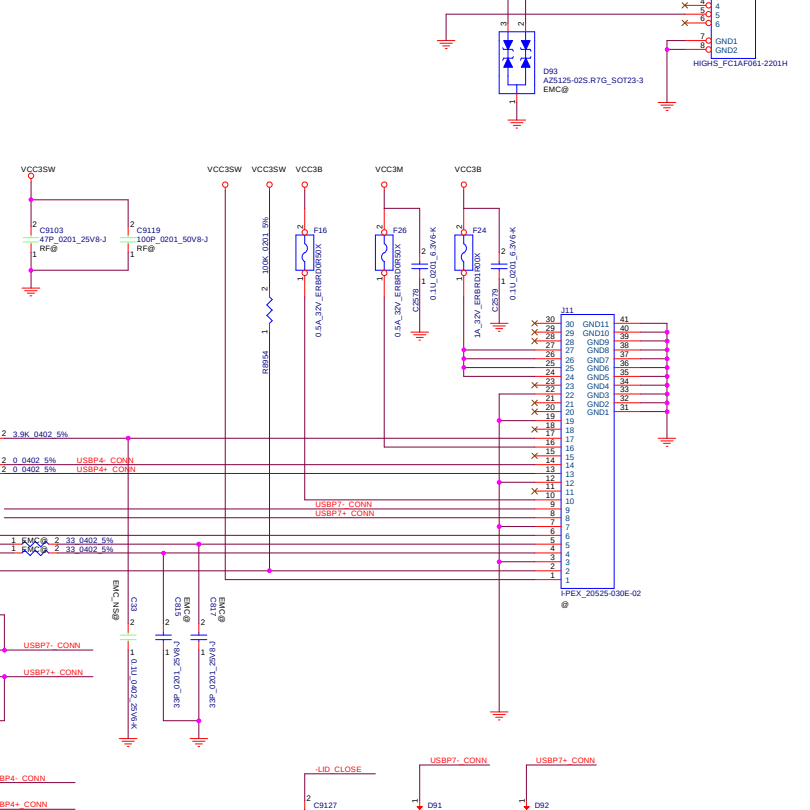
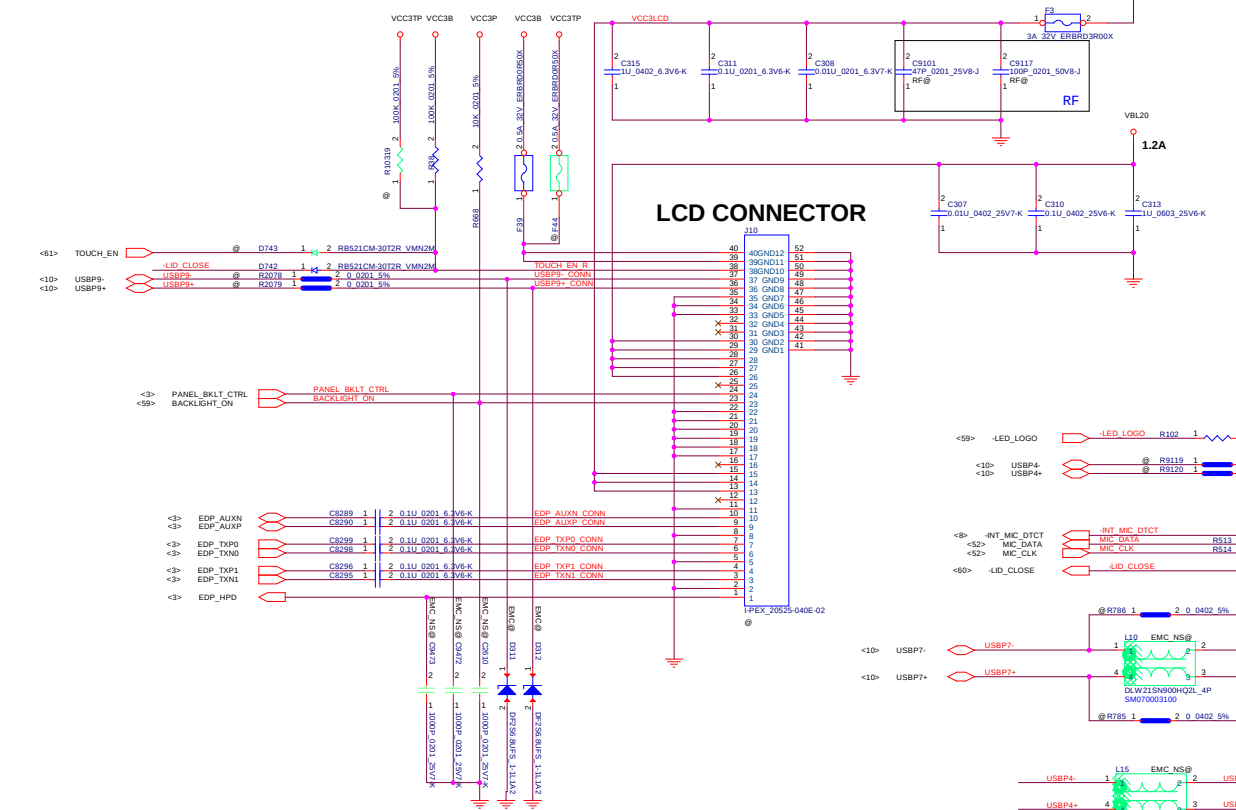
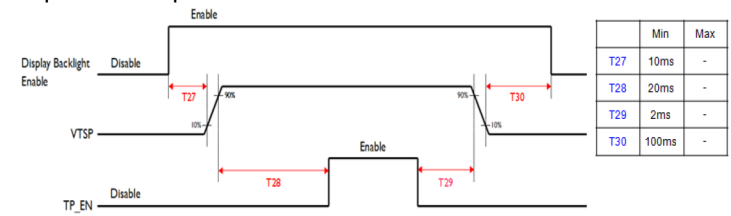


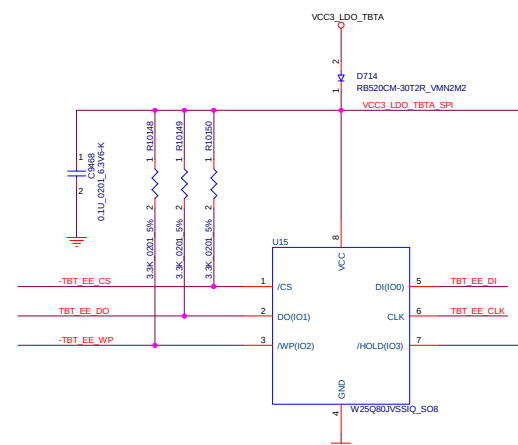
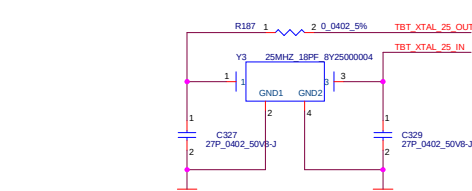
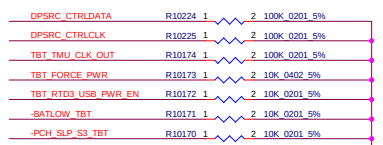
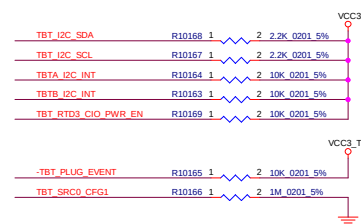
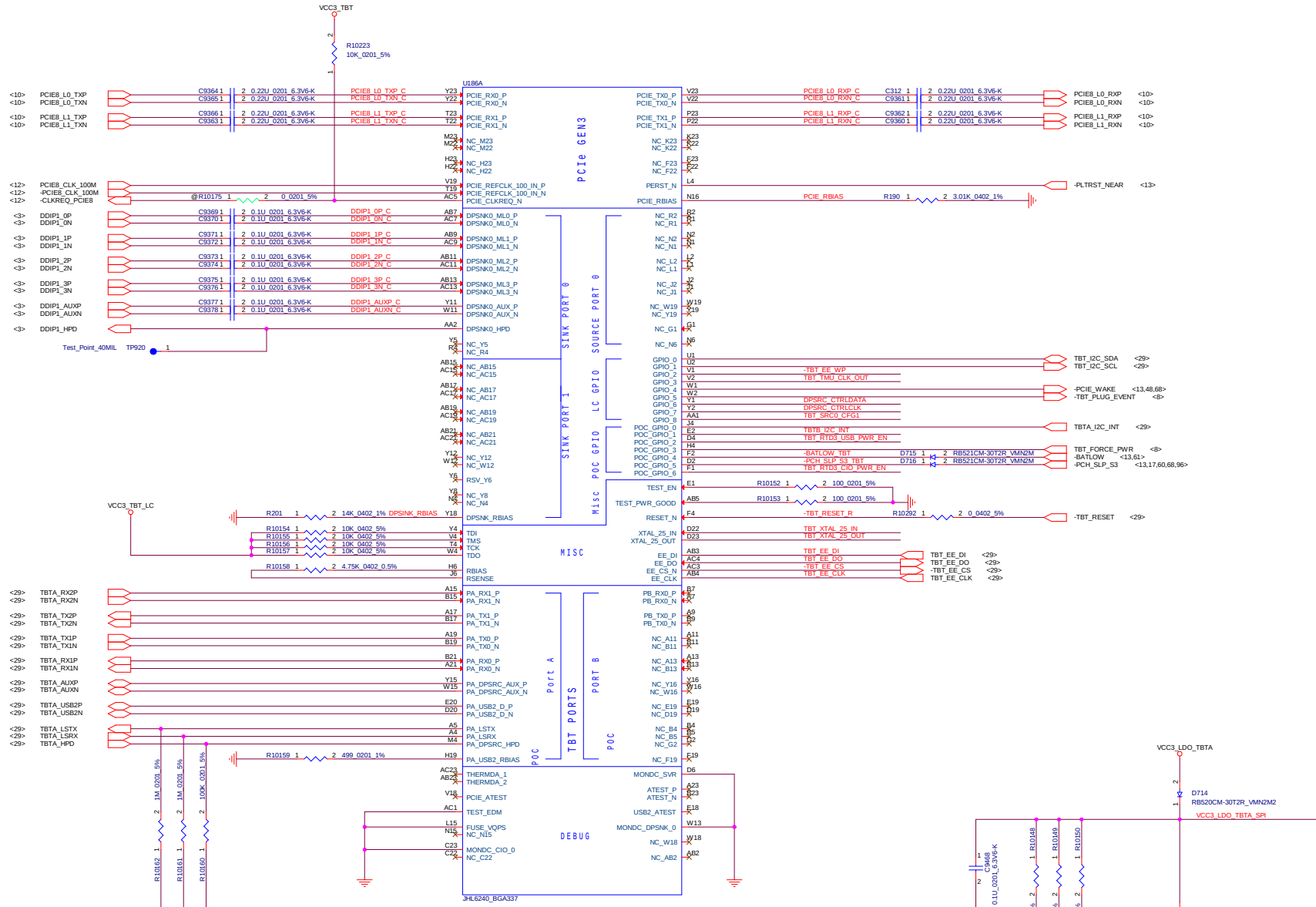
Touch Panel Sequence		
	Support	Non-Support
R10319	ASM	No ASM
F44	ASM	No ASM
D743	ASM	No ASM
Q266	ASM	No ASM
R10321	ASM	No ASM
C9487	ASM	No ASM
R10320	ASM	No ASM
D744	ASM	No ASM
R10322	ASM	No ASM
R10323	ASM	No ASM
R38	No ASM	ASM
F39	No ASM	ASM
R10307	No ASM	ASM
R2412	No ASM	ASM

Page 01  
Page 01  
Page 01  
Page 01



# TP power on/off Sequence:





Y3 CRYSTAL 25MHZ 18PF 30PPM			
Vendor	P/N	LCFC P/N	
TXC	8Y25000004	SJ10000H00J	
KDS	1ZZHAE25000CC0F	SJ10000P300	

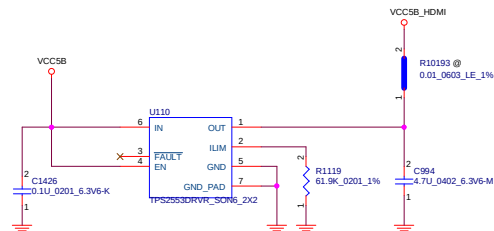
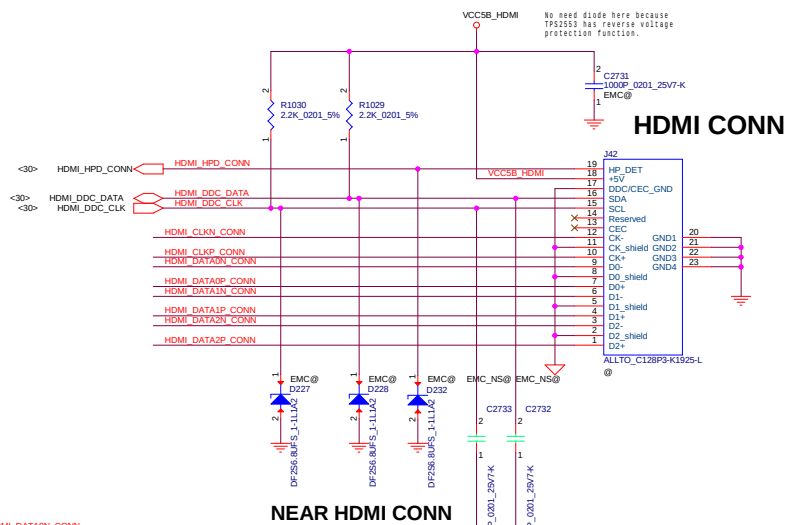
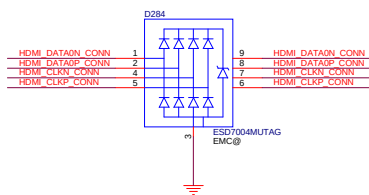
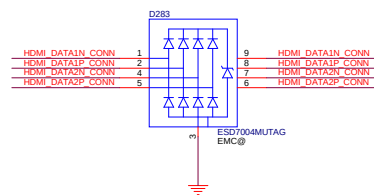
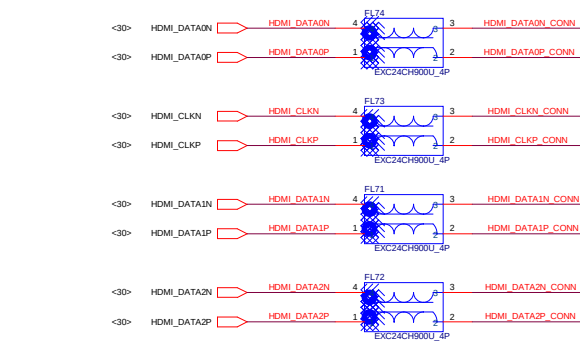
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**TABLE: PI3EQX862 Input Equalization Setting (EQ\_A & EQ\_B)**

	@3GHz	@4GHz
GND	7 dB	8 dB
Open	4 dB (Default)	5 dB (Default)
VDD	10 dB	11 dB

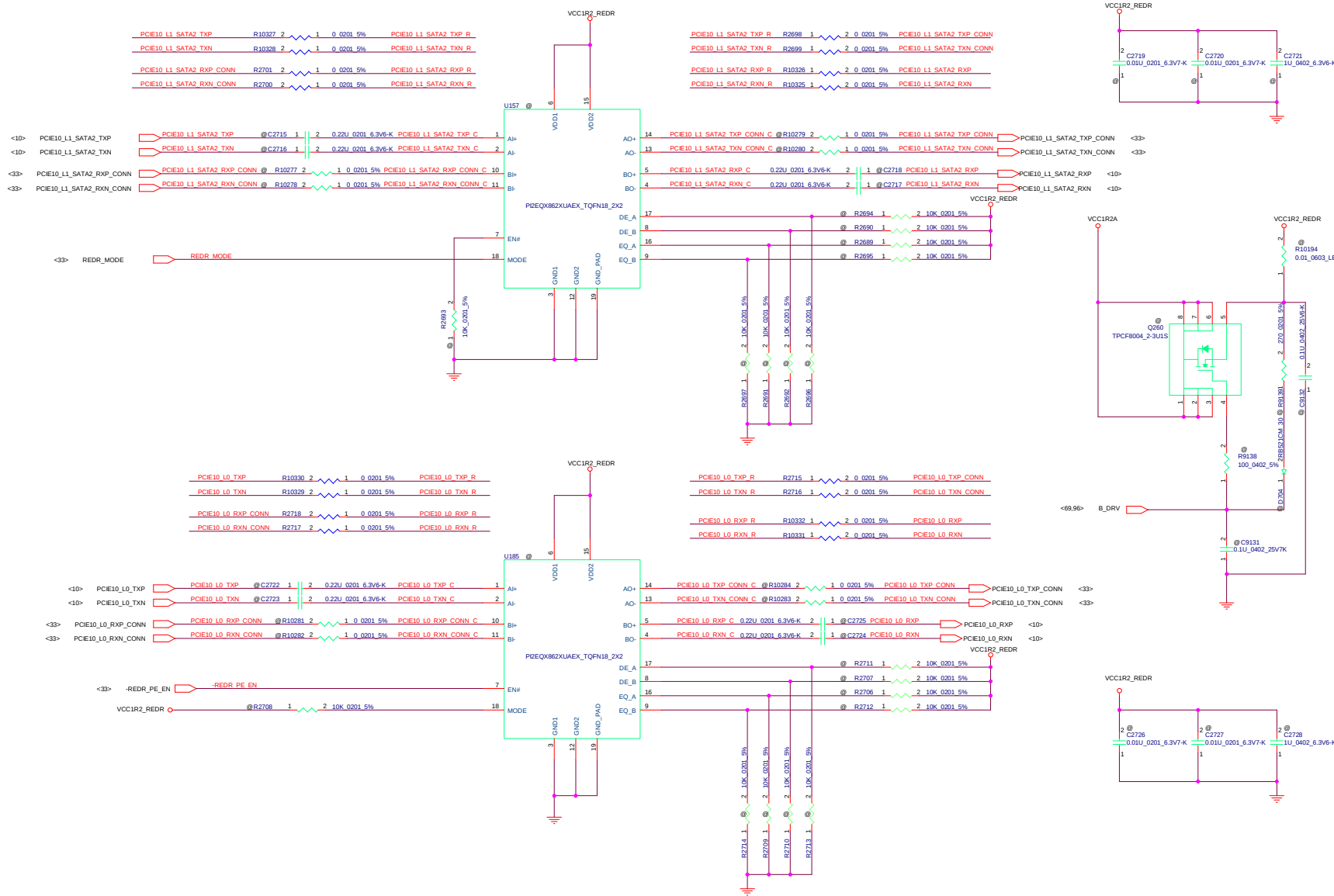
**TABLE: PI3EQX862 Output De-emphasis Setting (DE\_A & DE\_B)**

GND	-2.5 dB
Open	0 dB (Default)
VDD	-4 dB

← LOGIC

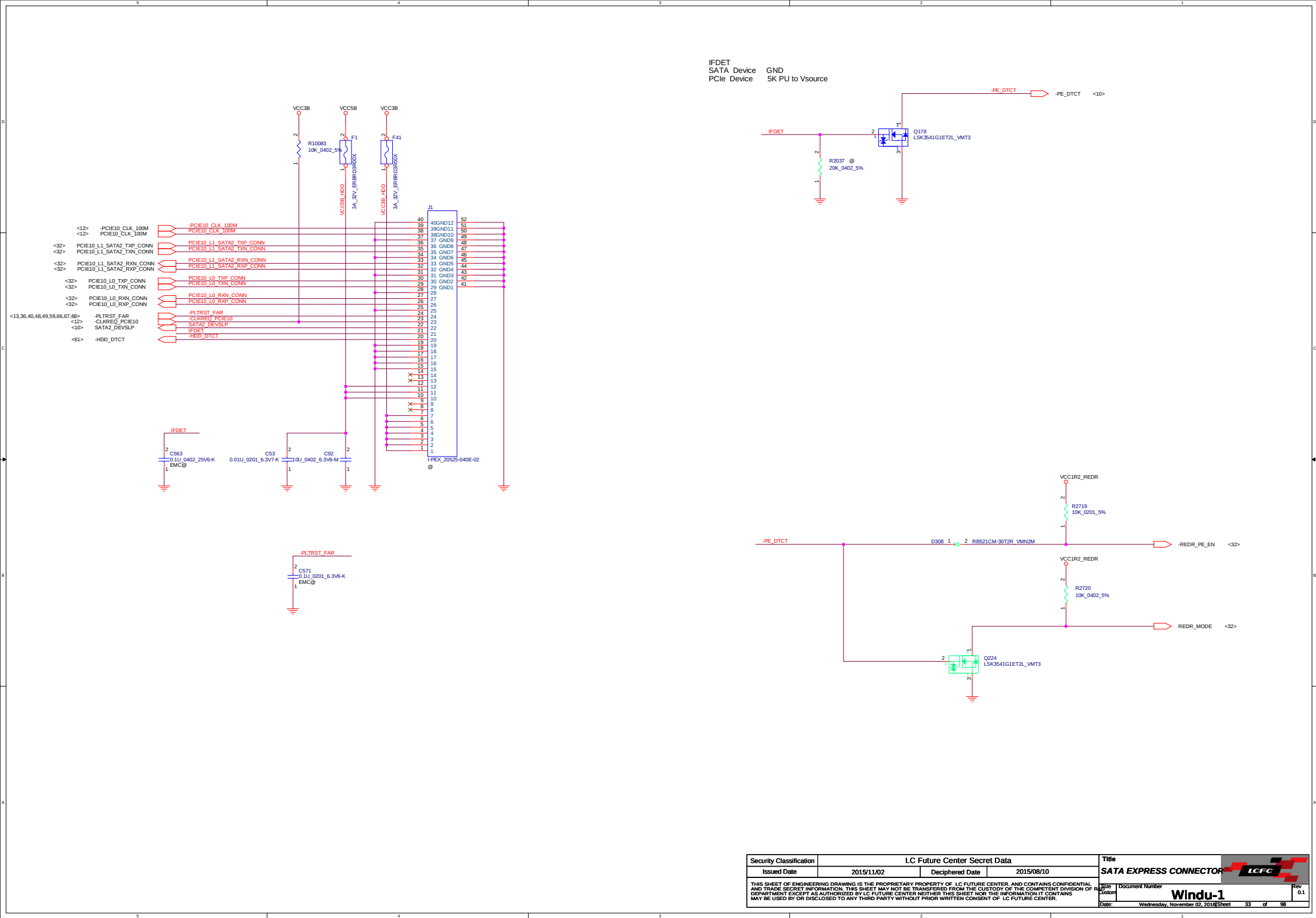
**TABLE: Mode Configuration Table**

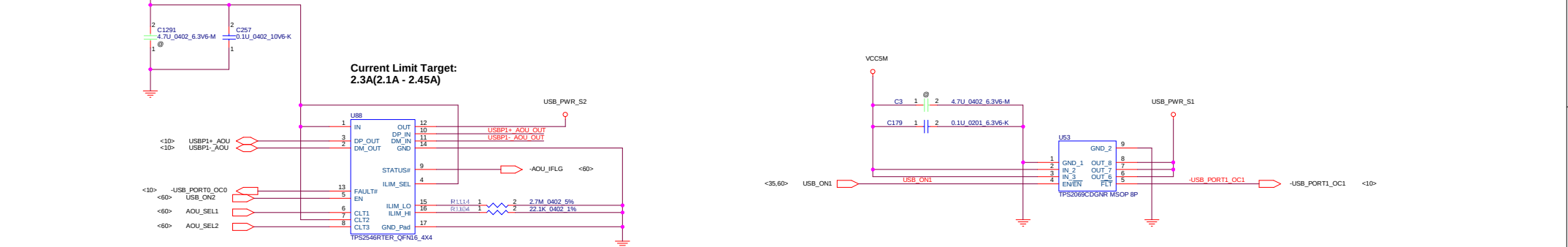
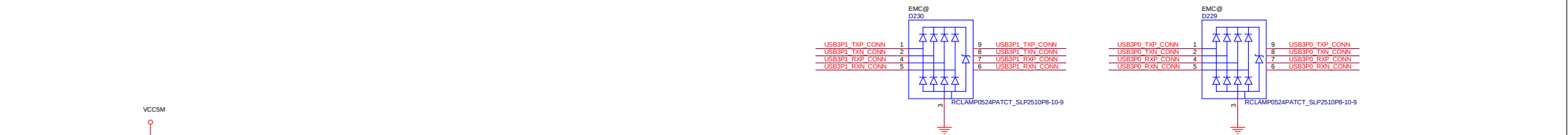
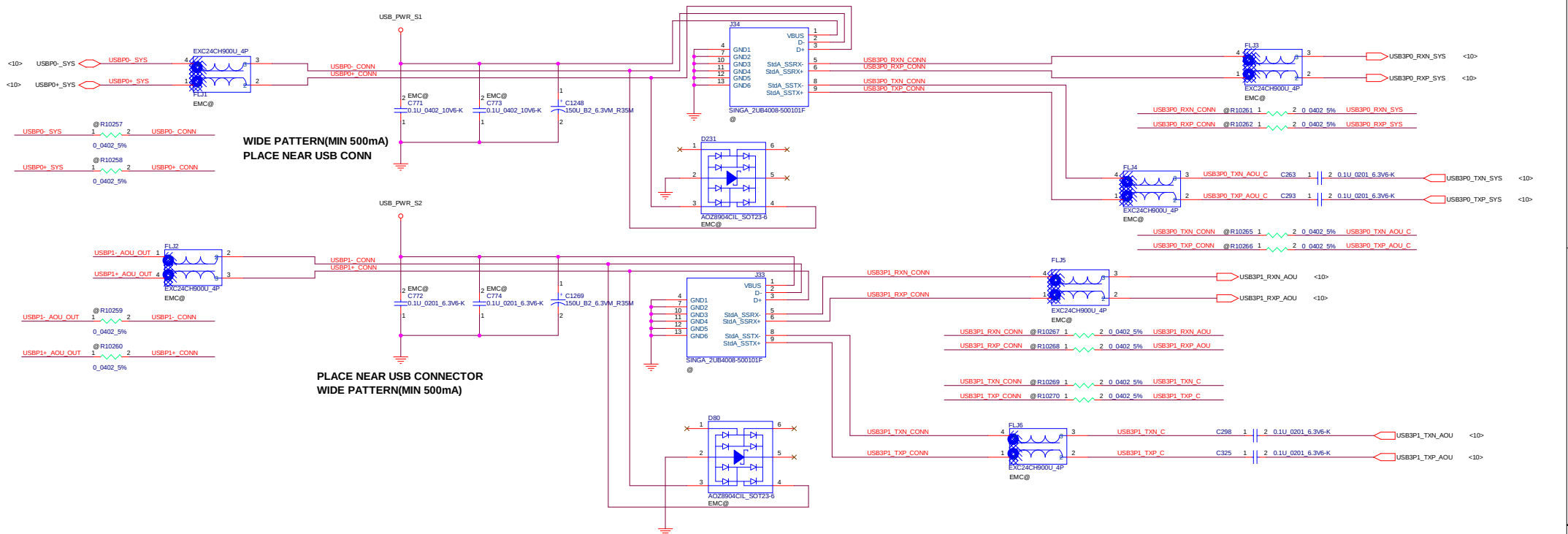
EN#	MODE	Mode
Low	Low	SATA Application
Low	High	PCIe Application
High	X	Disable



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Title			
STORAGE I/F REDRIVER			
Size Custom	Document Number	Rev 0	
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Vendor	P/N	LCFC P/N
TI	TPS2546RTER	SA00005TD00
Pericom	PI5USB2546ZHEX	SA000066I00

Vendor	P/N	LCFC P/N
TI	TPS2069CDGMR	SA00005TE00
Rohm	BD82032FVJ-GE2	SA000084S00

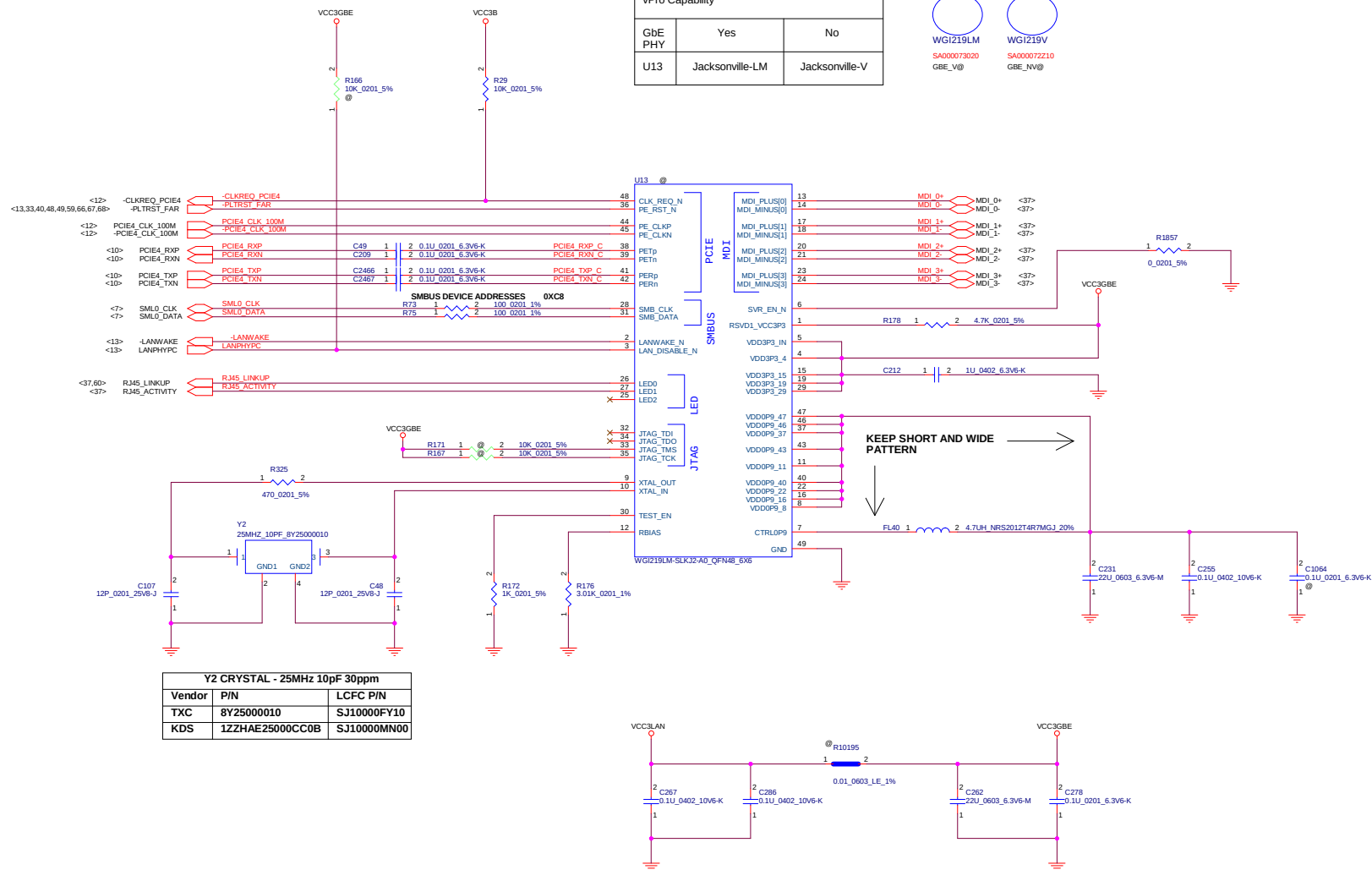


TABLE

vPro Capability		
GbE PHY	Yes	No
U13	Jacksonville-LM	Jacksonville-V

U13  
WG1219LM  
SA000073020  
GBE\_V@

U13  
WG1219V  
SA000072210  
GBE\_NV@





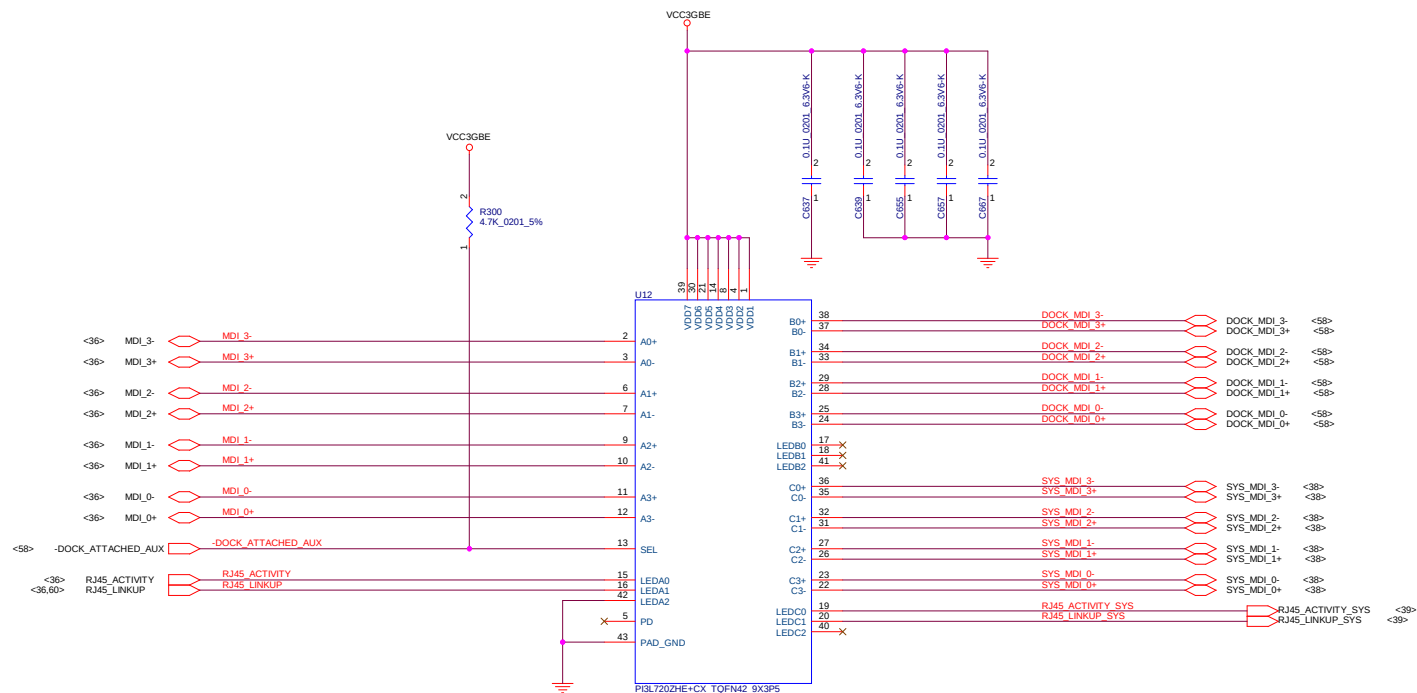
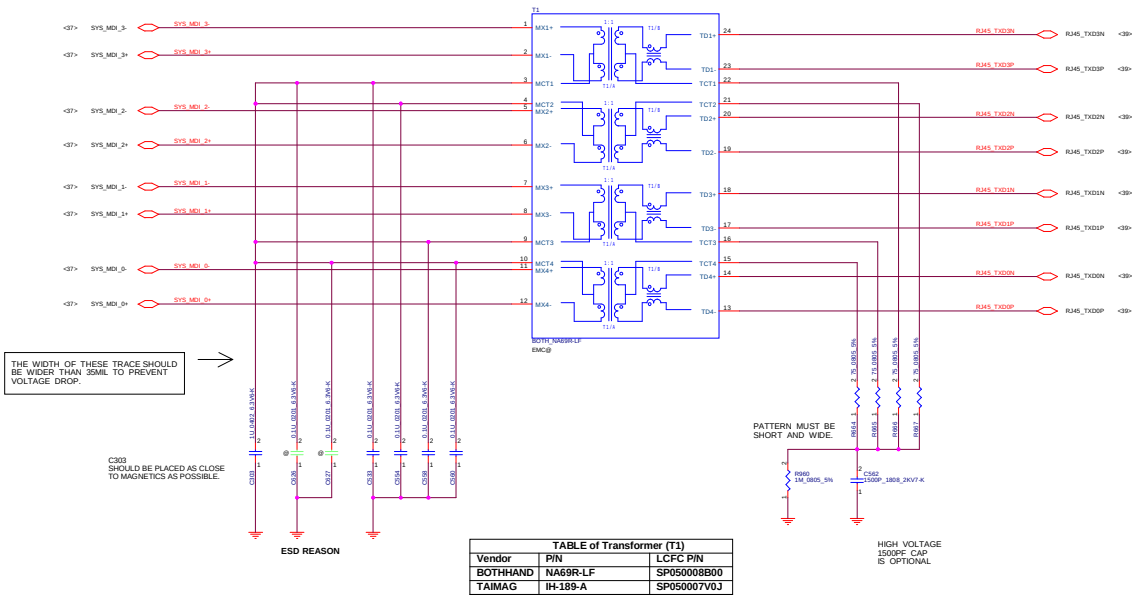
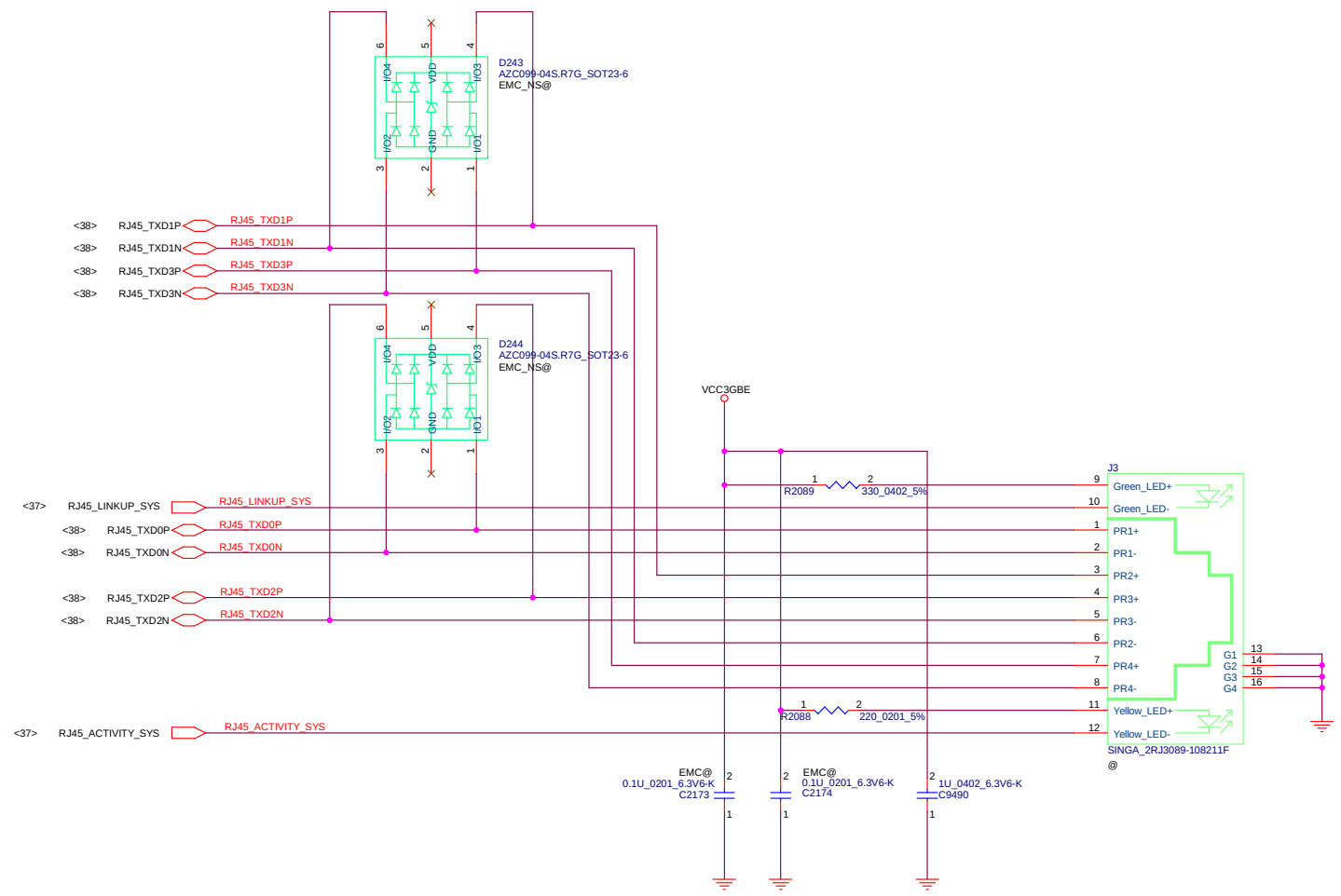
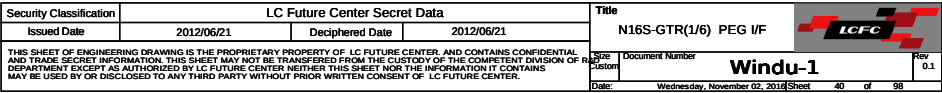


TABLE of LAN Switch (U12)		
Vendor	P/N	LCFC P/N
PERICOM	PI3L720ZHE+CX	SA00007E900
TI	TS3L501ERUAR	SA000072400





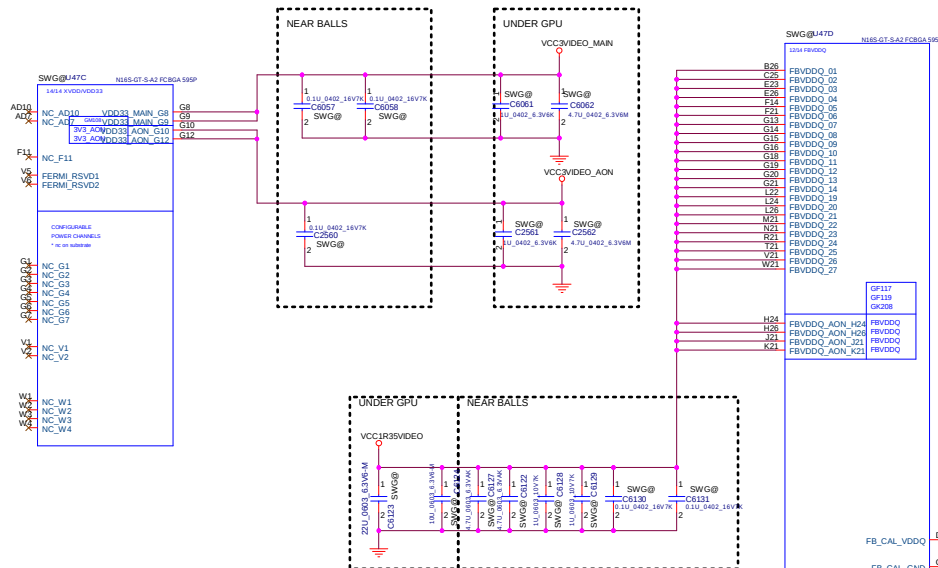
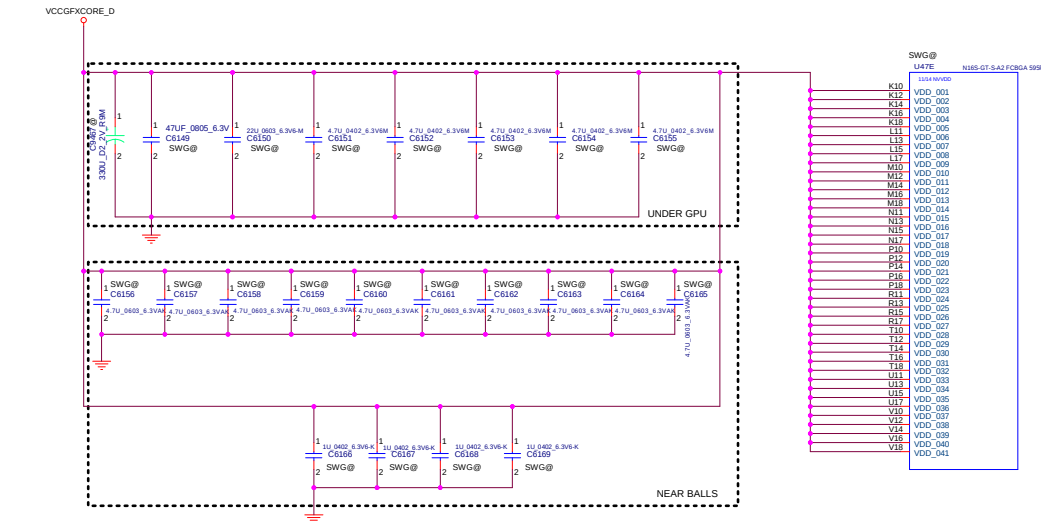




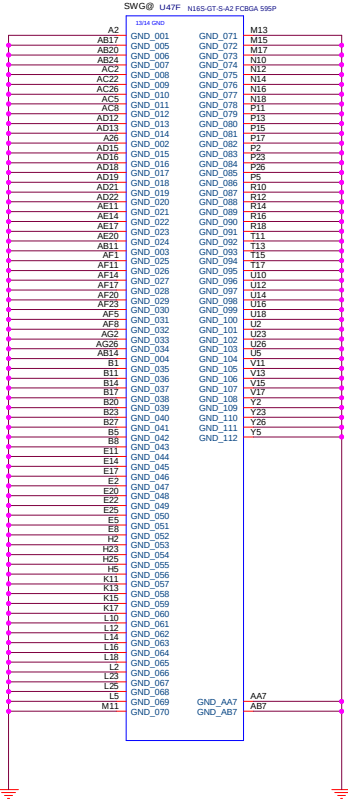
A vertical number line with four points labeled A, B, C, and D from bottom to top. An arrow points to point C.

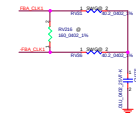
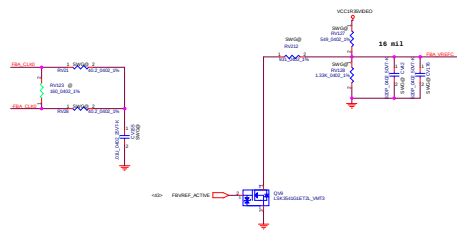
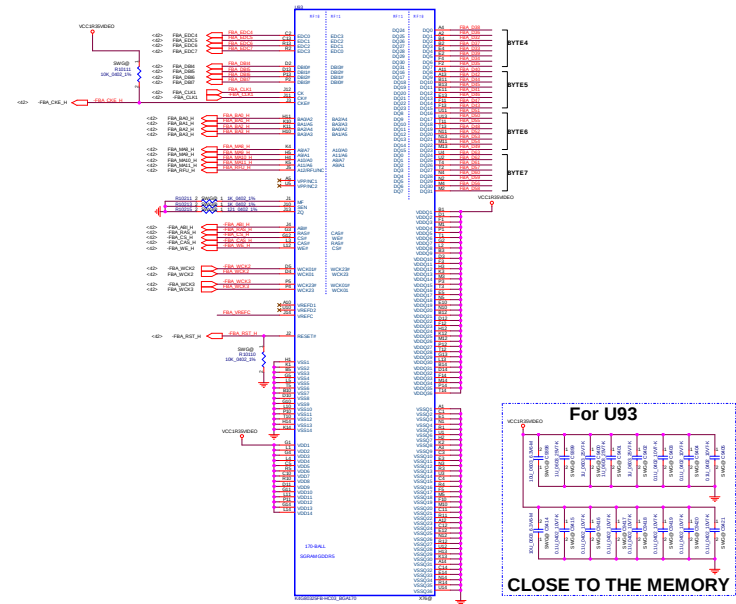











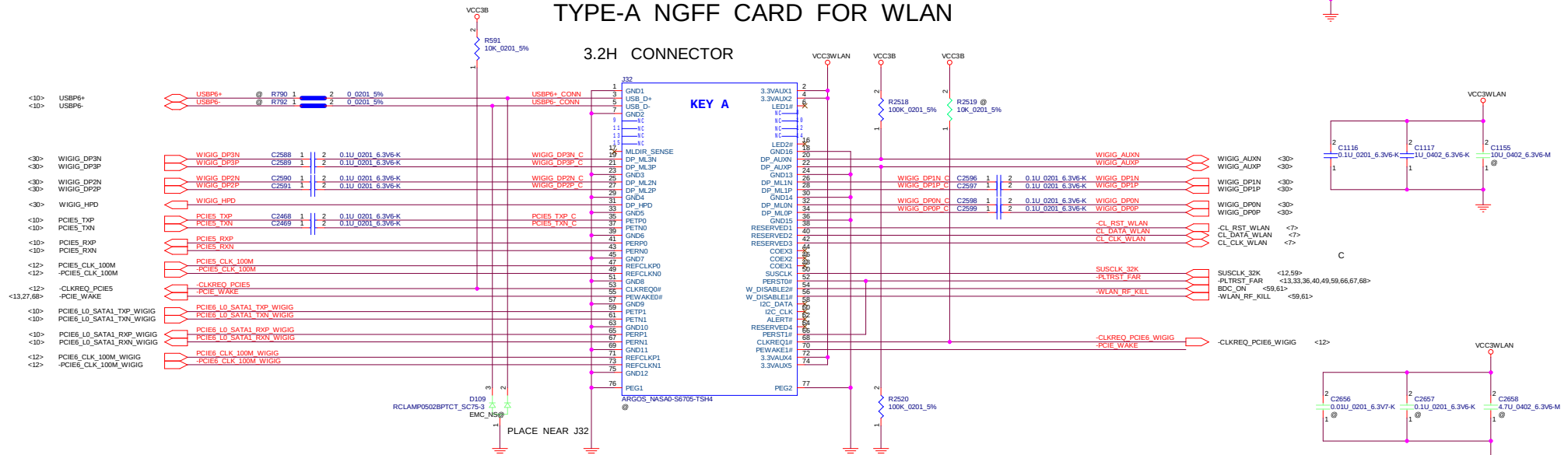



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Issued Date	2012/05/02	Deciphered Date	2012/5/02	<b>MEMORY TERMINATION</b>	
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# TYPE-A NGFF CARD FOR WLAN

3.2H CONNECTOR

KEY A



Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/11/02	Deciphered Date	2015/08/10	S-2 SOCKET 1 MODULE I/F			
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Size		Document Number		Rev		0.1	
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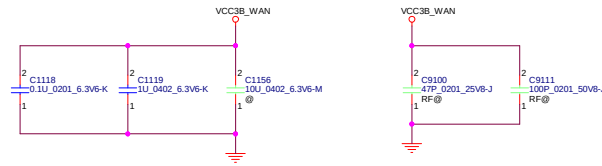
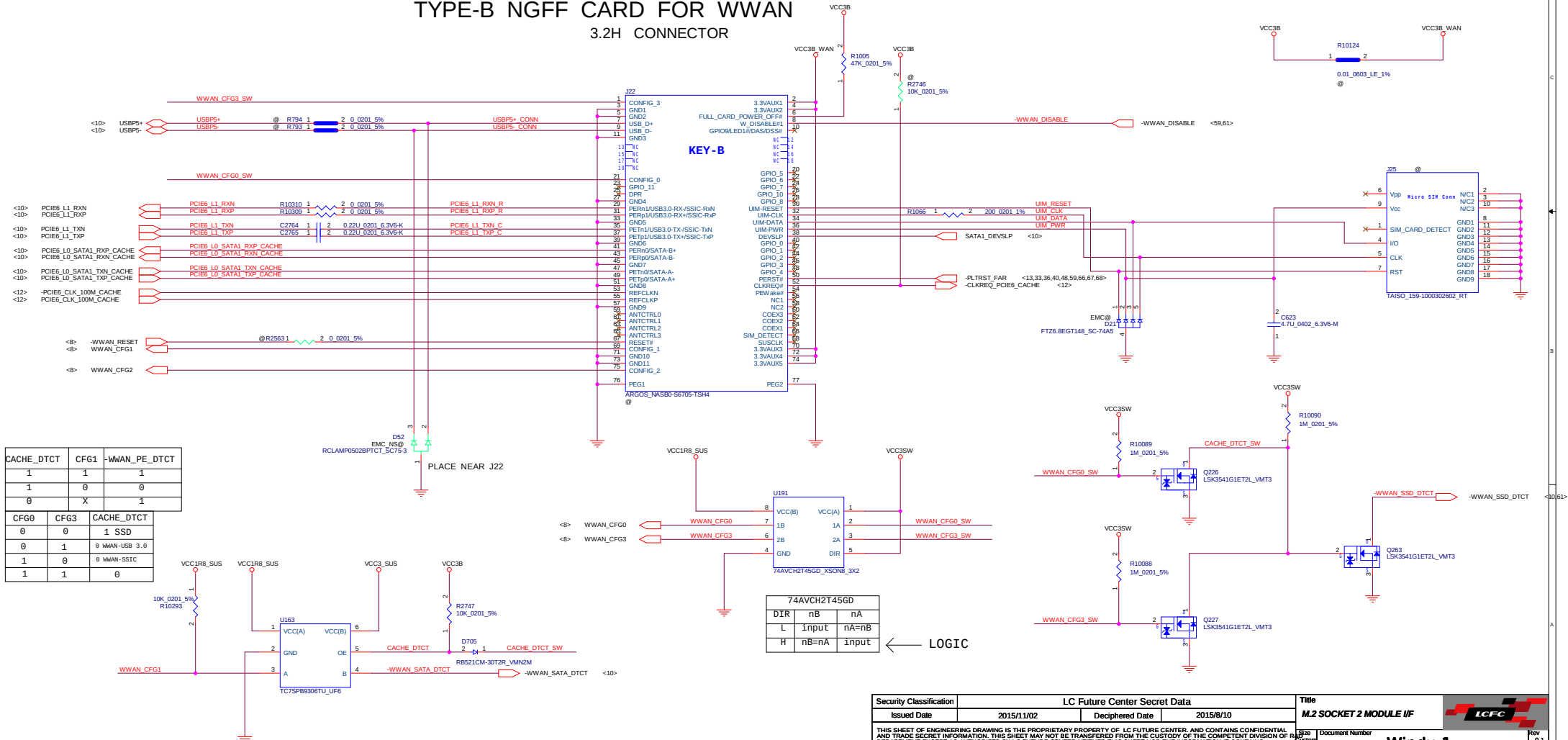
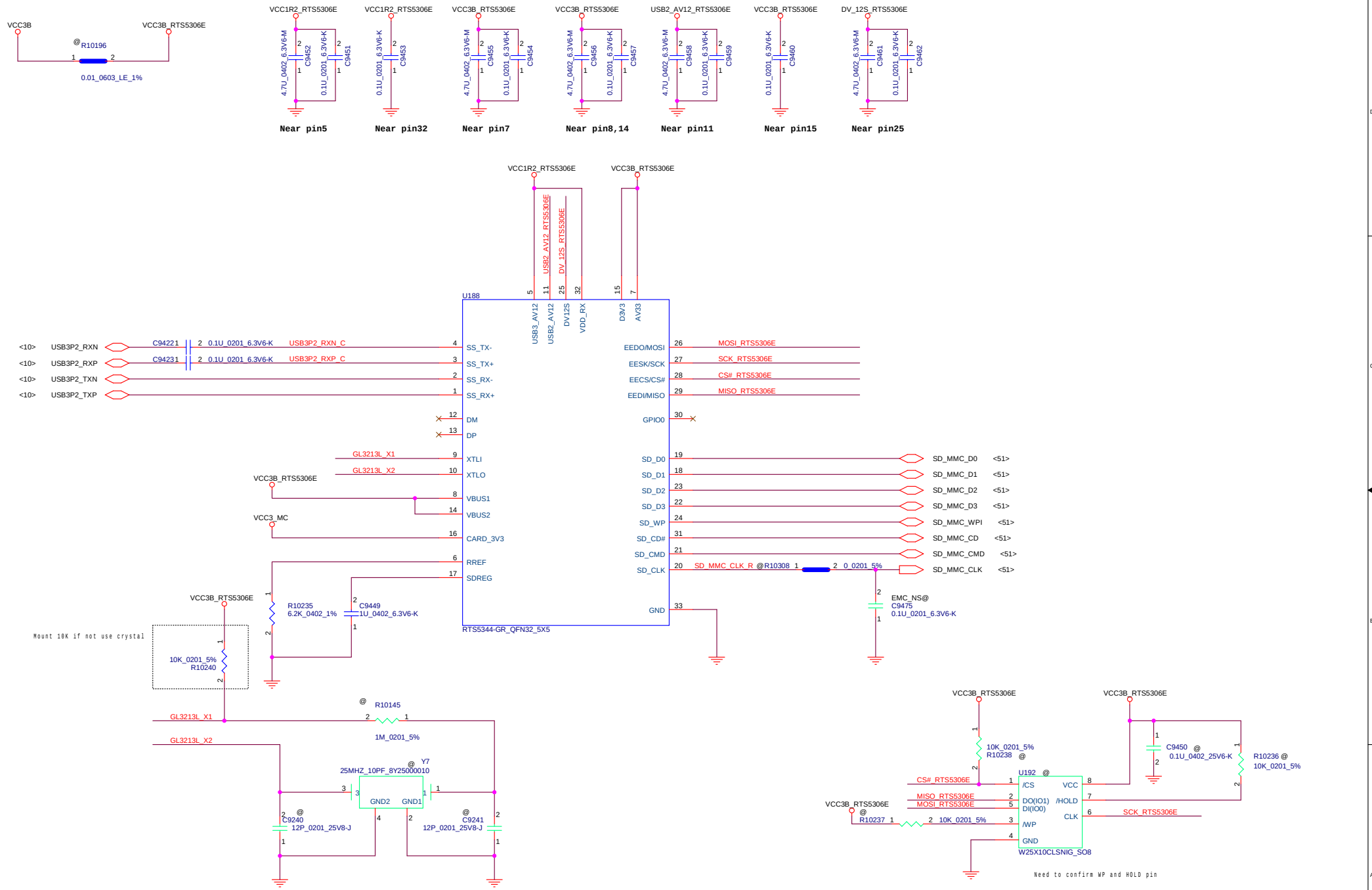


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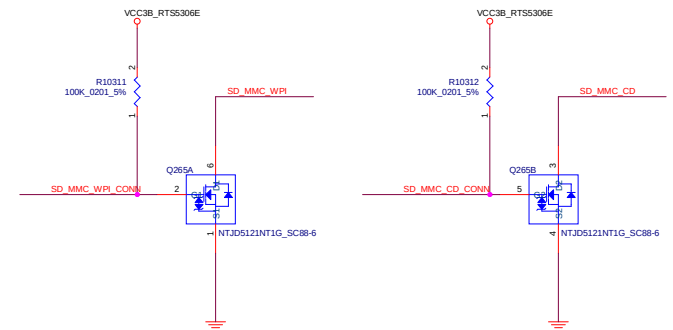
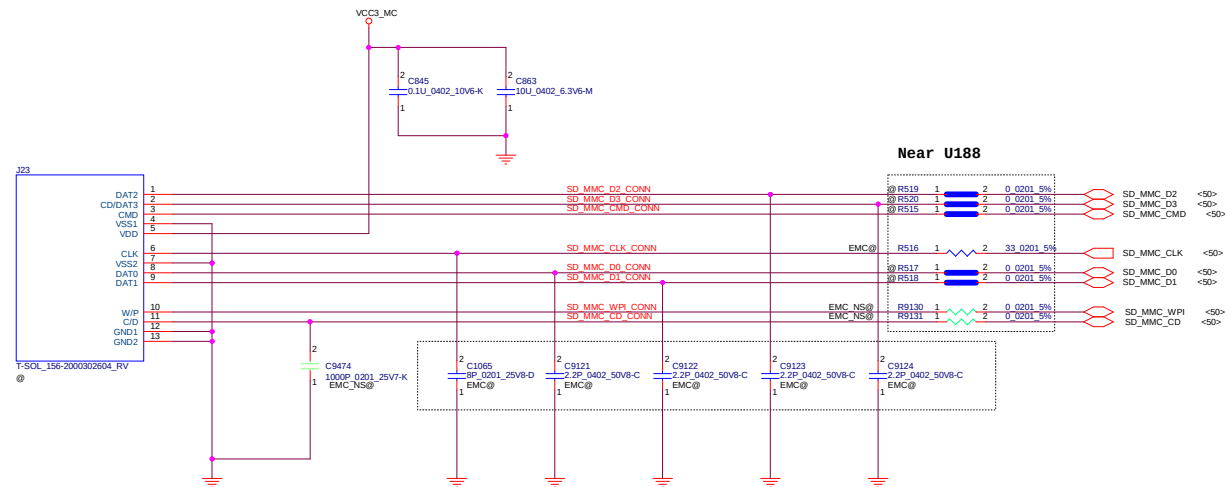
State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG 0 (Pin 21)	CONFIG 3 (Pin 1)	CONFIG 2 (Pin 75)	CONFIG 1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - USB 3.0	0
5	GND	NC	GND	NC	WWAN - USB 3.0	1
6	GND	NC	NC	GND	WWAN - USB 3.0	2
7	GND	NC	NC	NC	WWAN - USB 3.0	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A

## TYPE-B NGFF CARD FOR WWAN 3.2H CONNECTOR





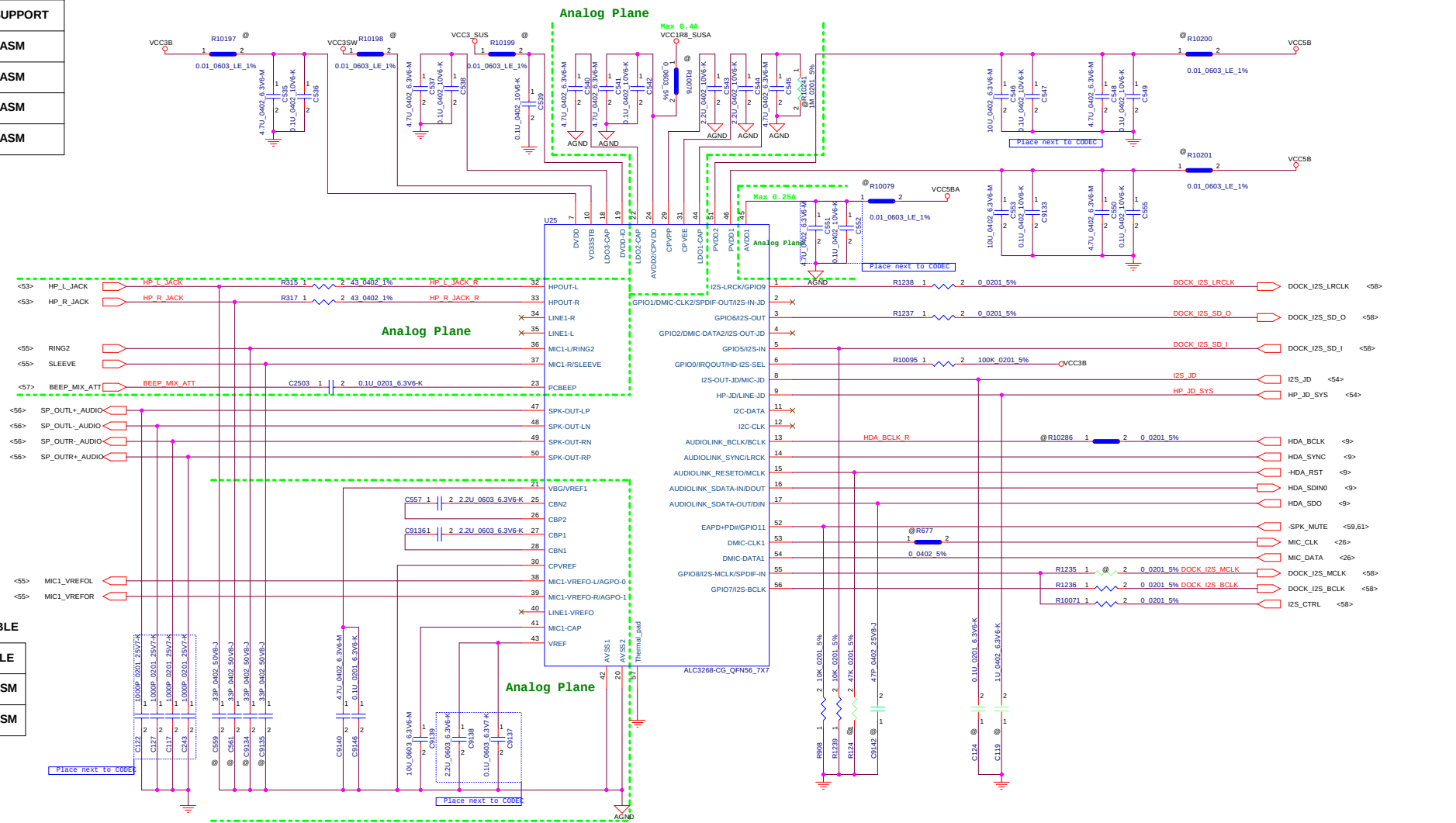
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/11/02	Deciphered Date	2015/8/10	MEDIA CARD CONTROLLER	
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				Rev	0.1



TABLE

Dock support		
	SUPPORT	NON-SUPPORT
R1235	NO ASM	NO ASM
R1236	ASM	NO ASM
R1237	ASM	NO ASM
R1238	ASM	NO ASM

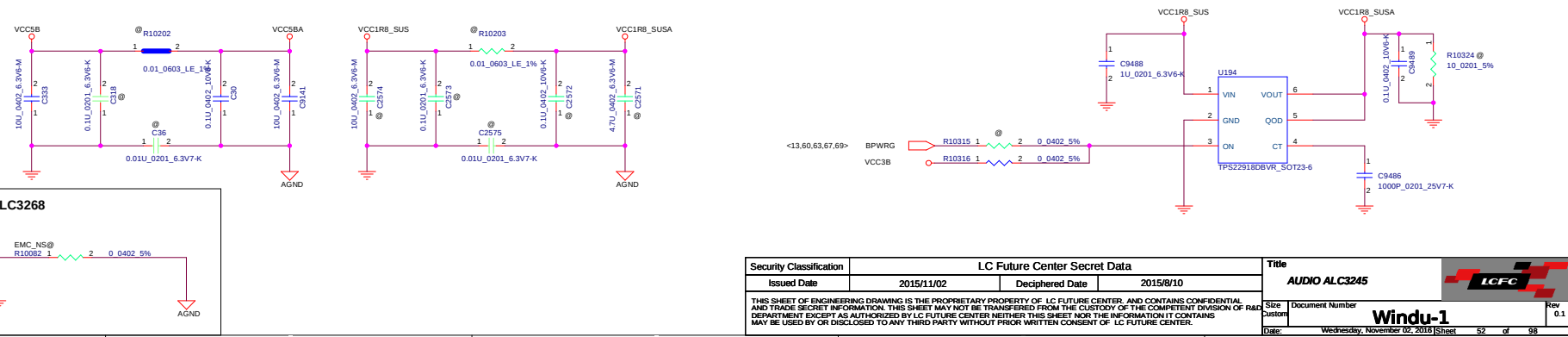
↑  
LOGIC




**TABLE MIC HW ENABLE/DISABLE**

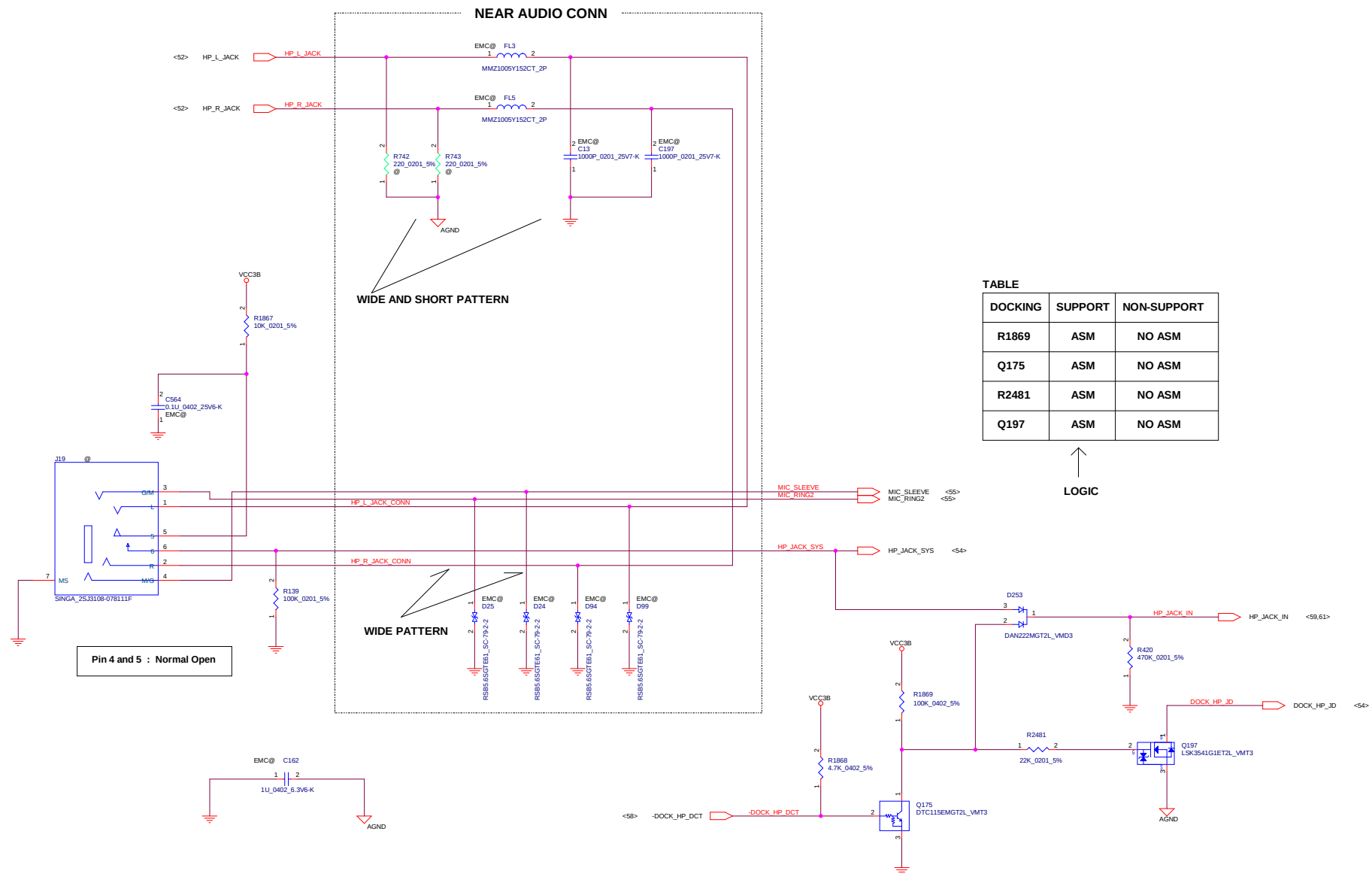
	ENABLE	DISABLE
R961	ASM	NO ASM
R677	ASM	NO ASM

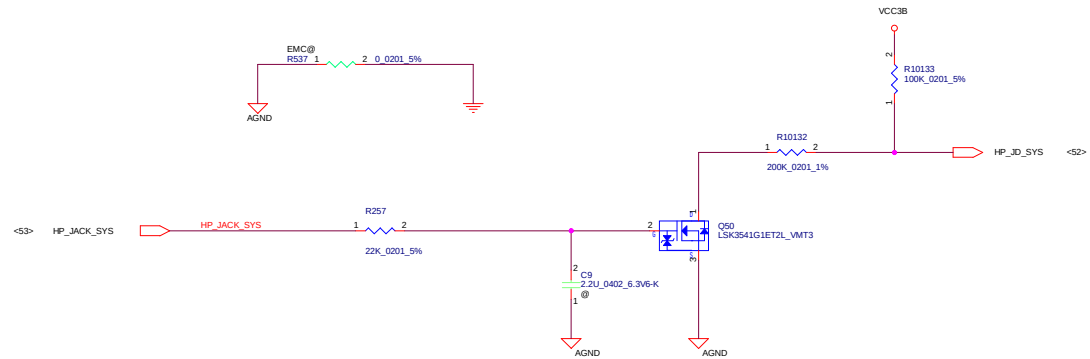
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LOGIC



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Issued Date		Deciphered Date		AUDIO AL3245	
2015/11/02		2015/8/10			
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Win10				0.1	
Date	Wednesday, November 02, 2014			Sheet 52 of 98	



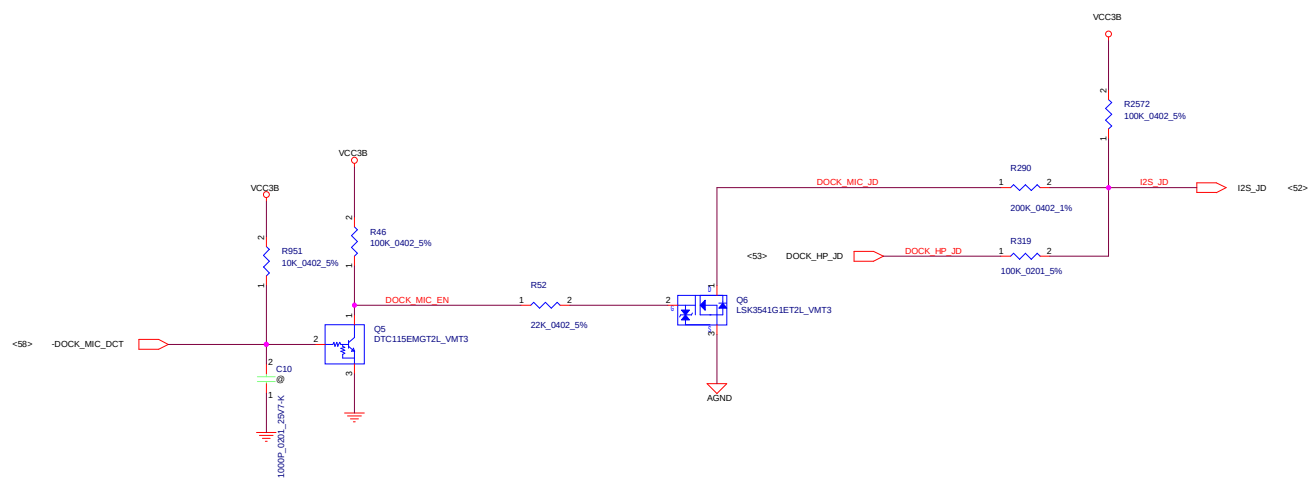


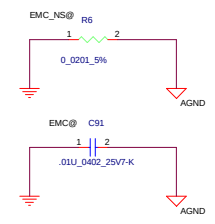
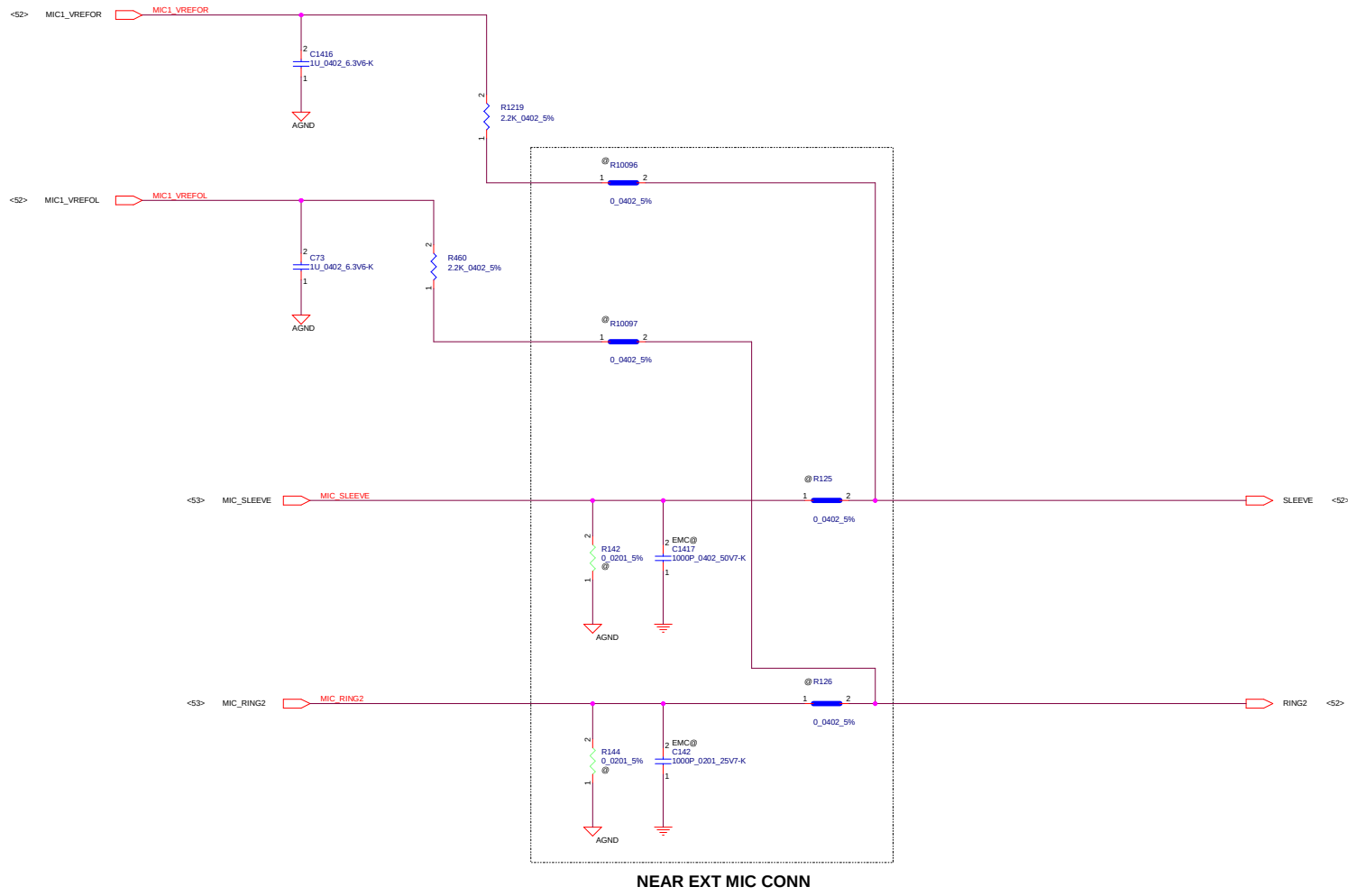


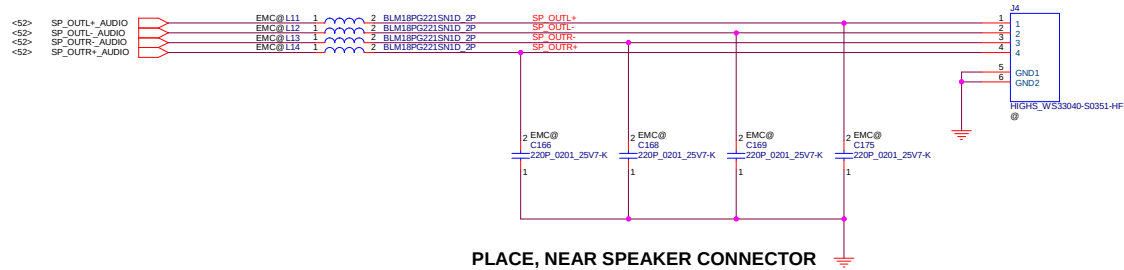
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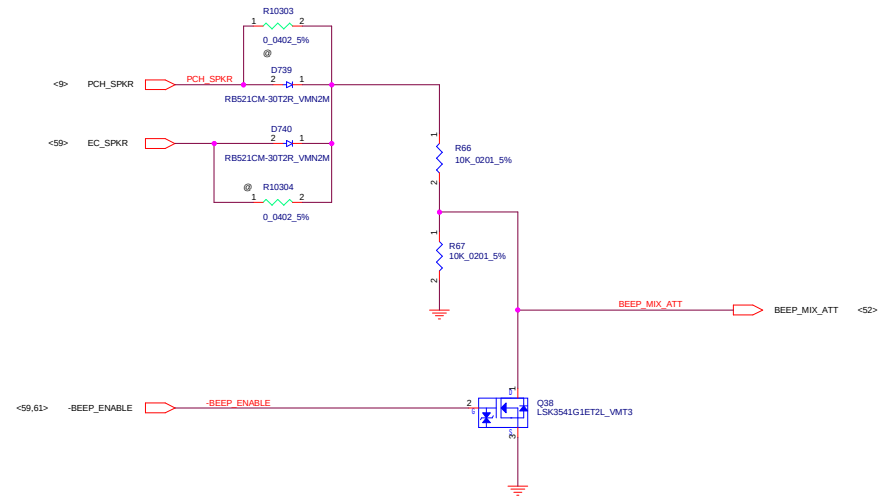
DOCKING	SUPPORT		NON SUPPORT
	MIC HW	ENABLE	DISABLE
R951	ASM	NO ASM	NO ASM
R290	ASM	NO ASM	NO ASM
R46	ASM	NO ASM	NO ASM
Q5	ASM	NO ASM	NO ASM
R52	ASM	NO ASM	NO ASM
Q6	ASM	NO ASM	NO ASM
R319	ASM	ASM	NO ASM
R2572	ASM	ASM	NO ASM


↑  
LOGIC





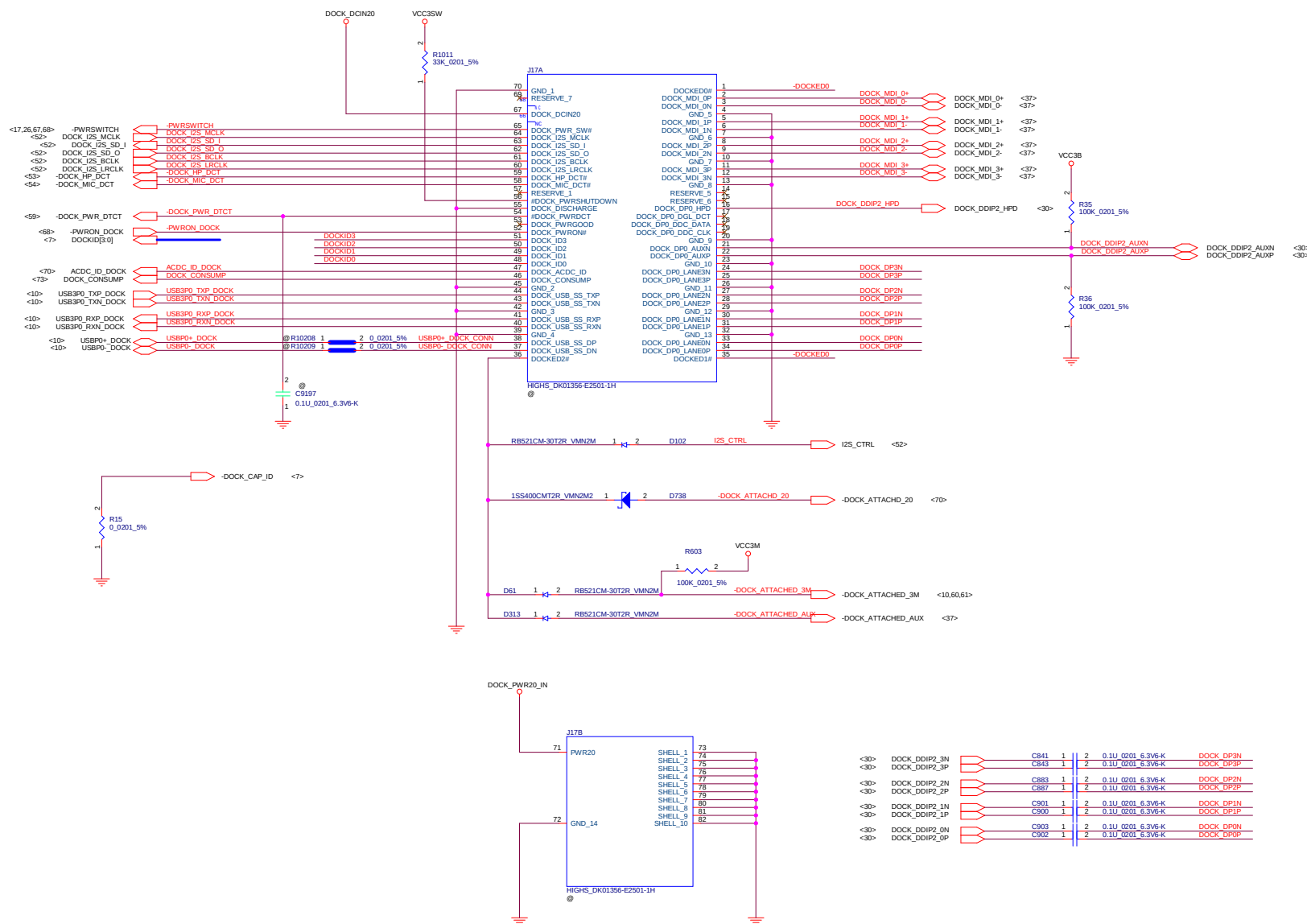






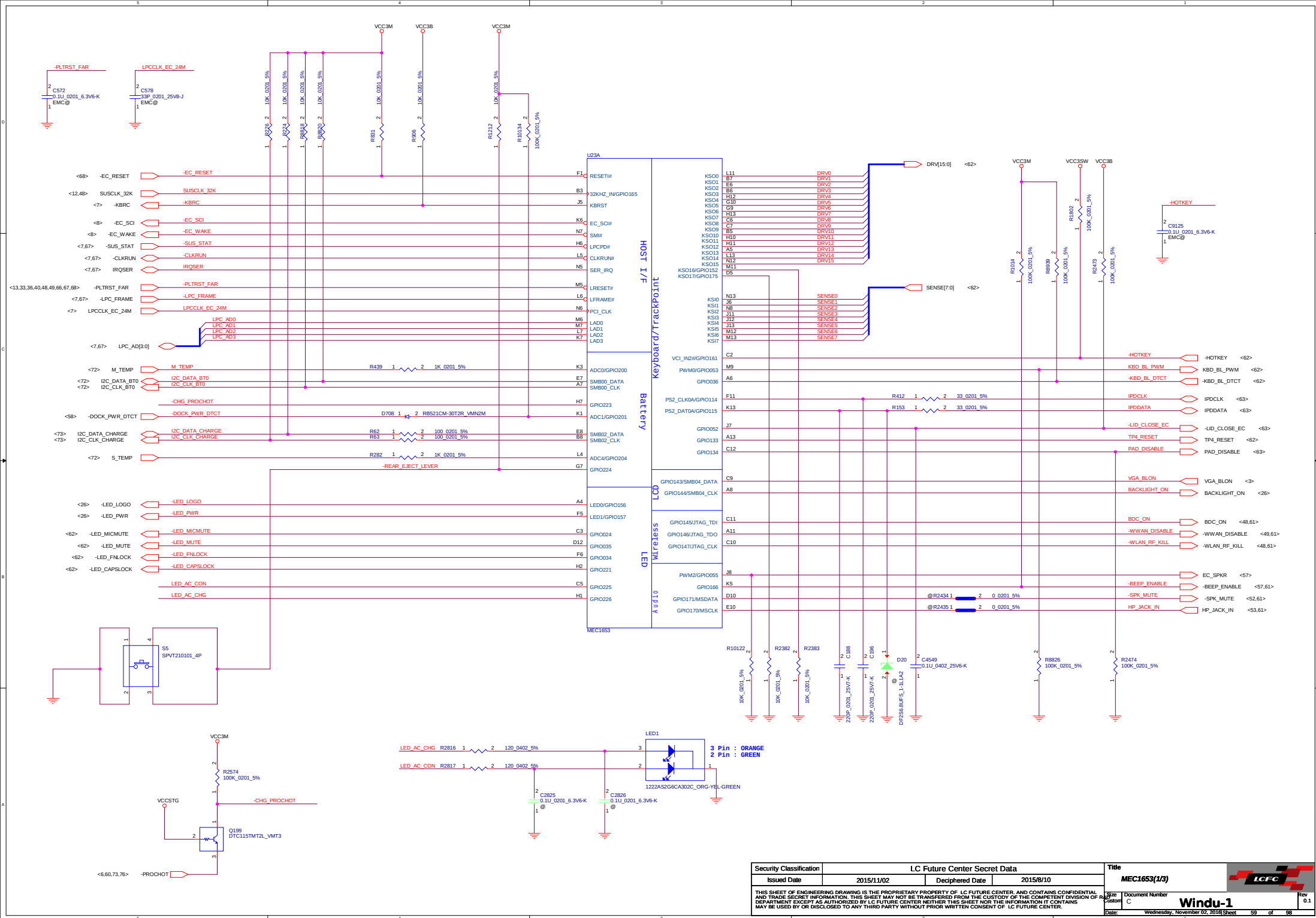
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Issued Date	2015/11/02	Deciphered Date	2015/8/10	AUDIO BEEP			
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Revision		Document Number		C		Rev 0.1	
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<div>LOGIC</div> <div>↓</div>		
TABLE		
ID	DOCKING SUPPORT	NON-SUPPORT
J17	ASM	NO ASM
R1011	ASM	NO ASM
D2	ASM	NO ASM
R603	ASM	ASM
D61	ASM	NO ASM
D102	ASM	NO ASM
C24	ASM	NO ASM
Q85	ASM	NO ASM
R95	ASM	NO ASM
R731	ASM	NO ASM
R657	ASM	NO ASM
C841	ASM	NO ASM
C843	ASM	NO ASM
C883	ASM	NO ASM
C887	ASM	NO ASM
C901	ASM	NO ASM
C900	ASM	NO ASM
C903	ASM	NO ASM
C902	ASM	NO ASM
R35	ASM	NO ASM
R36	ASM	NO ASM
R15	ASM	NO_ASM



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Issued Date	2015/11/02	Deciphered Date	2015/8/10	DOCKING CONNECTOR			
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**MEC1653**

**Power Management**

**Thermal**

**USB/AUX**

**TABLE**

Sensor	Device	Placed on
DIODE0	EC internal	TOP
DIODE1	CPU DC/DC	BOTTOM
DIODE2	WWAN	BOTTOM
DIODE3	WLAN	BOTTOM
DIODE4	FAN	BOTTOM
DIODE5	dGPU DC/DC	BOTTOM
DIODE6	DIMM	BOTTOM

**Security Classification**

**LC Future Center Secret Data**

**Title**

**MEC1653(2/3)**

**Issued Date**

**2015/11/02**

**Deciphered Date**

**2015/8/10**

**Size**

**Custom**

**Document Number**

**Windu-1**

**Date**

**Wednesday, November 02, 2016**

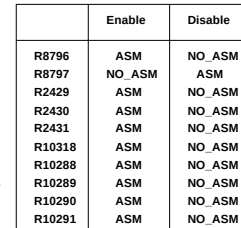
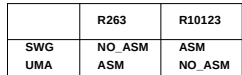
**Sheet**



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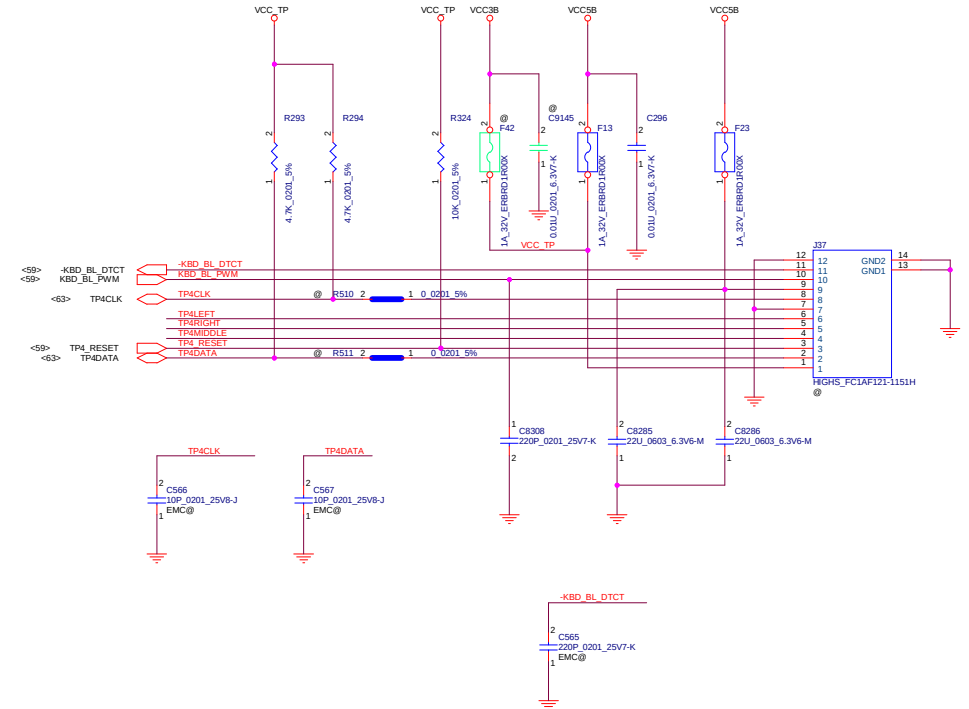
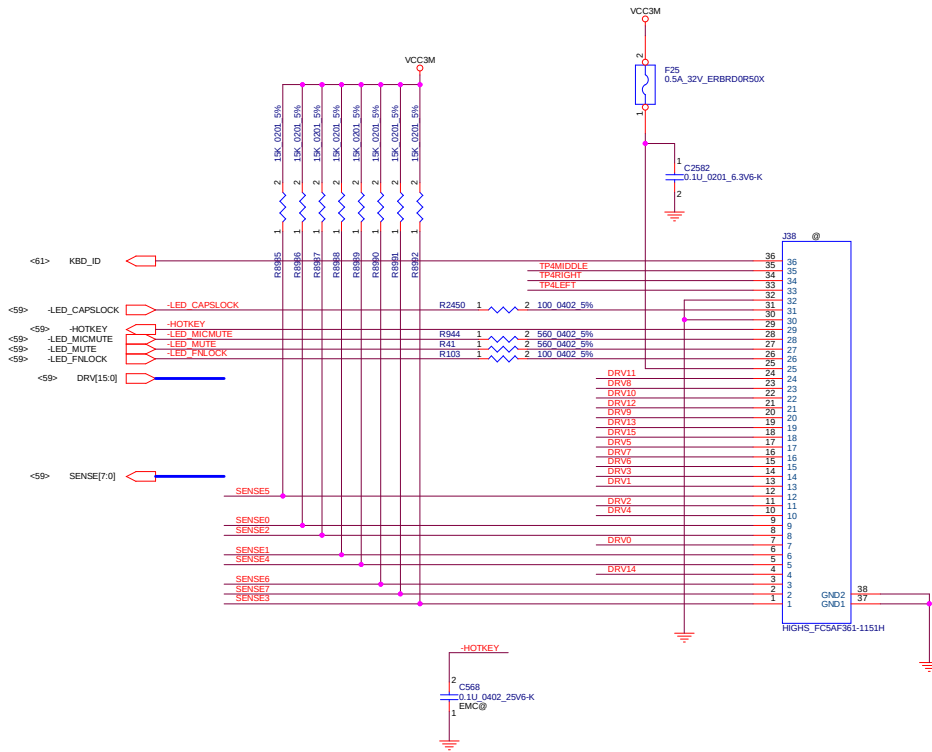
TABLE Sensor	Device	Placed on
DIODE0	EC internal	TOP
DIODE1	CPU DC/DC	BOTTOM
DIODE2	WWAN	BOTTOM
DIODE3	WLAN	BOTTOM
DIODE4	FAN	BOTTOM
DIODE5	dGPU DC/DC	BOTTOM
DIODE6	DIMM	BOTTOM



	Enable	Disable
R2434	22_5%	0_5%
R2435	22_5%	0_5%
R420	NO_ASM	ASM



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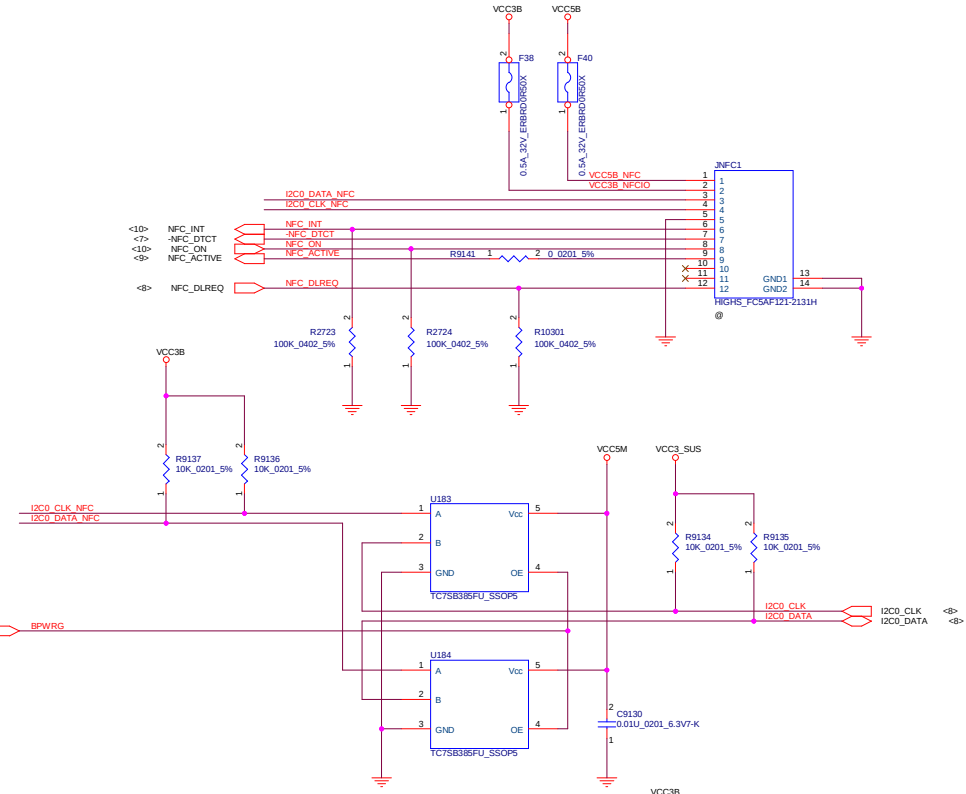
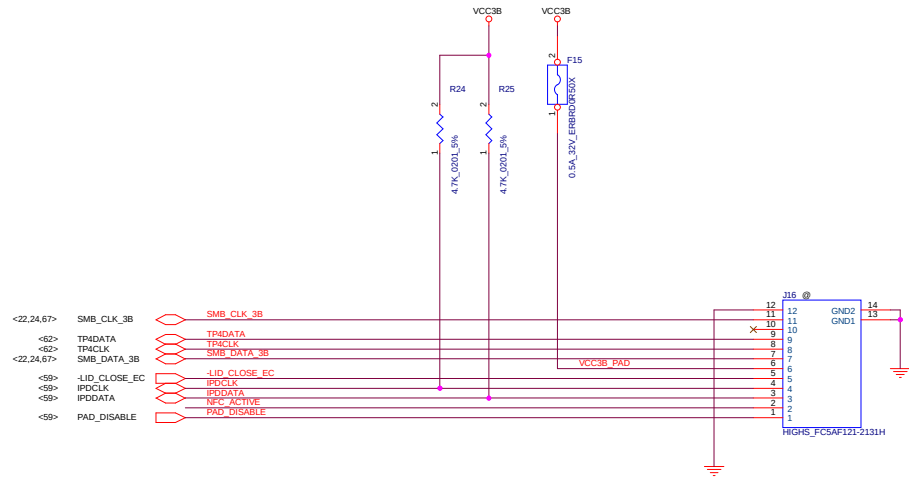
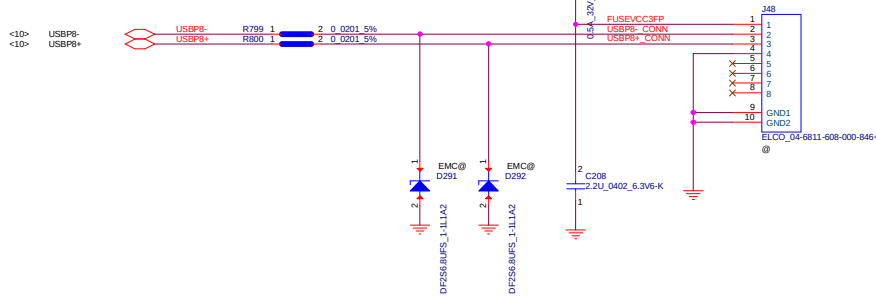
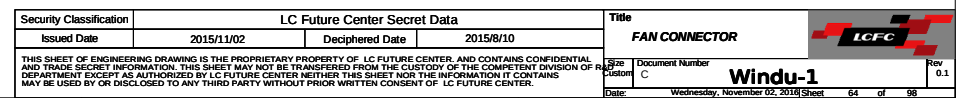


TABLE of U183/U184		
Vendor	P/N	LCFC P/N
TOSHIBA	TC7SB385FU	SA00005US0J
ON	7SB385DFT2G	SA00007CW00



PLACE NEAR J48



TABLE

P/N	ADDR_SEL	Address
BMA255	H	30h (W) & 31h (R)
	L	32h (W) & 33h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

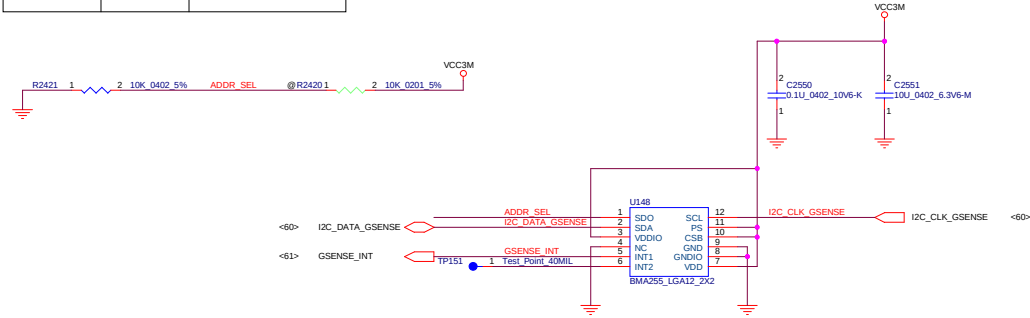
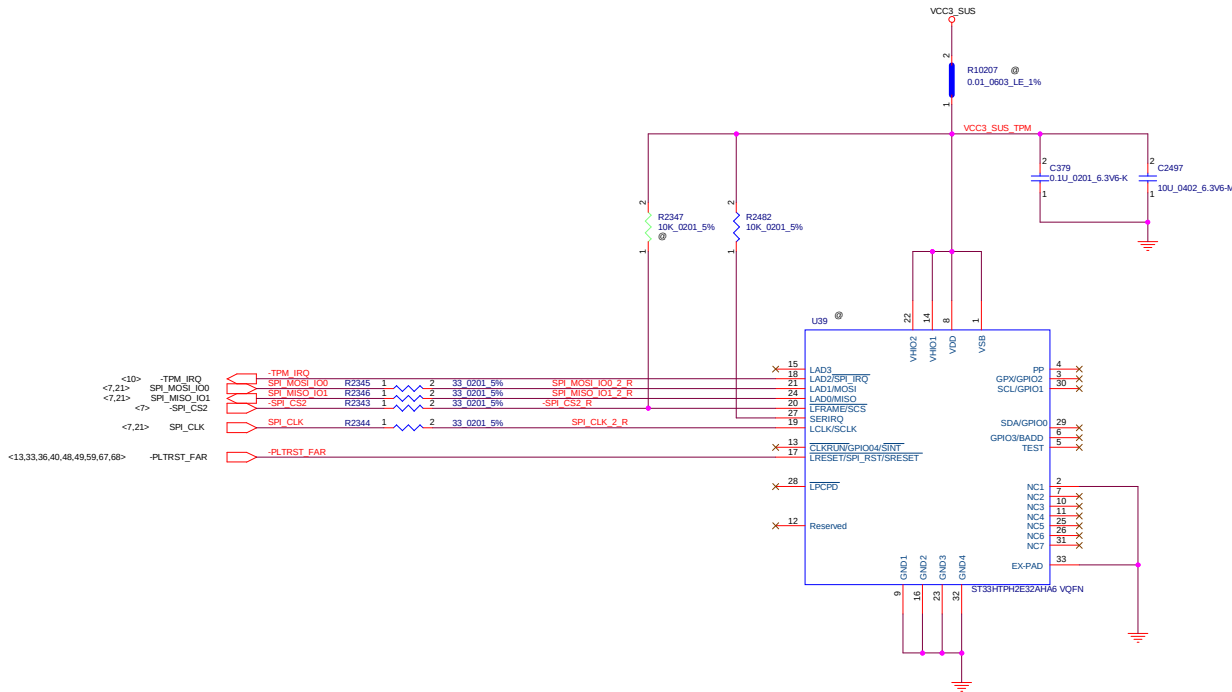


TABLE of G-Sensor (U148)		
Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00



TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.60 SA000075L20	ST Micro ST33HTPH2E32AH46 SA000081F00
1	VDD	VDD	NC
2	GND	GND	NC
3	GPIO	NC	NC
4	GPIO	NC	PP
5	NC	NC	NC
6	VNC/GPIO	GPIO	NC
7	GPIO/VDD	PP	GPIO
8	VDD	VDD	NC
9	GND	GND	NC
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	VNC/GPIO	NC	NC
14	VDD	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	VNC/GPIO	NC	NC
30	VNC/GPIO	NC	NC
31	VNC	NC	NC
32	GND	GND	NC

TPM2.0



TPM1.2



TABLE

REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

LOGIC

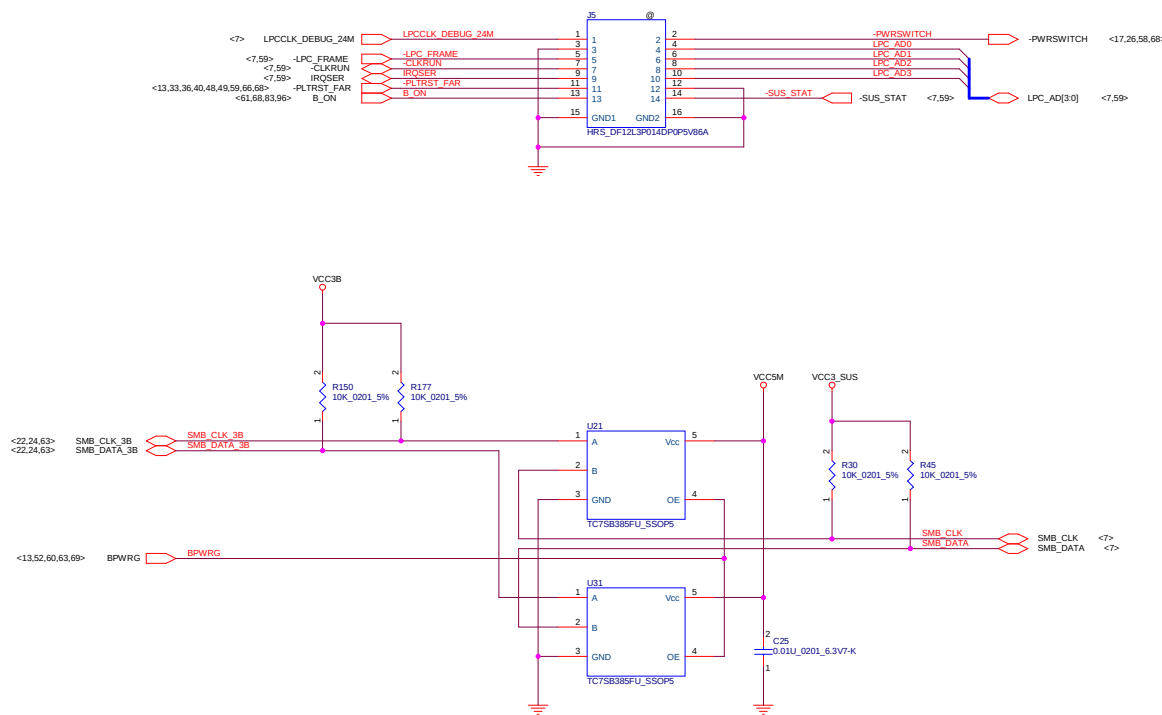
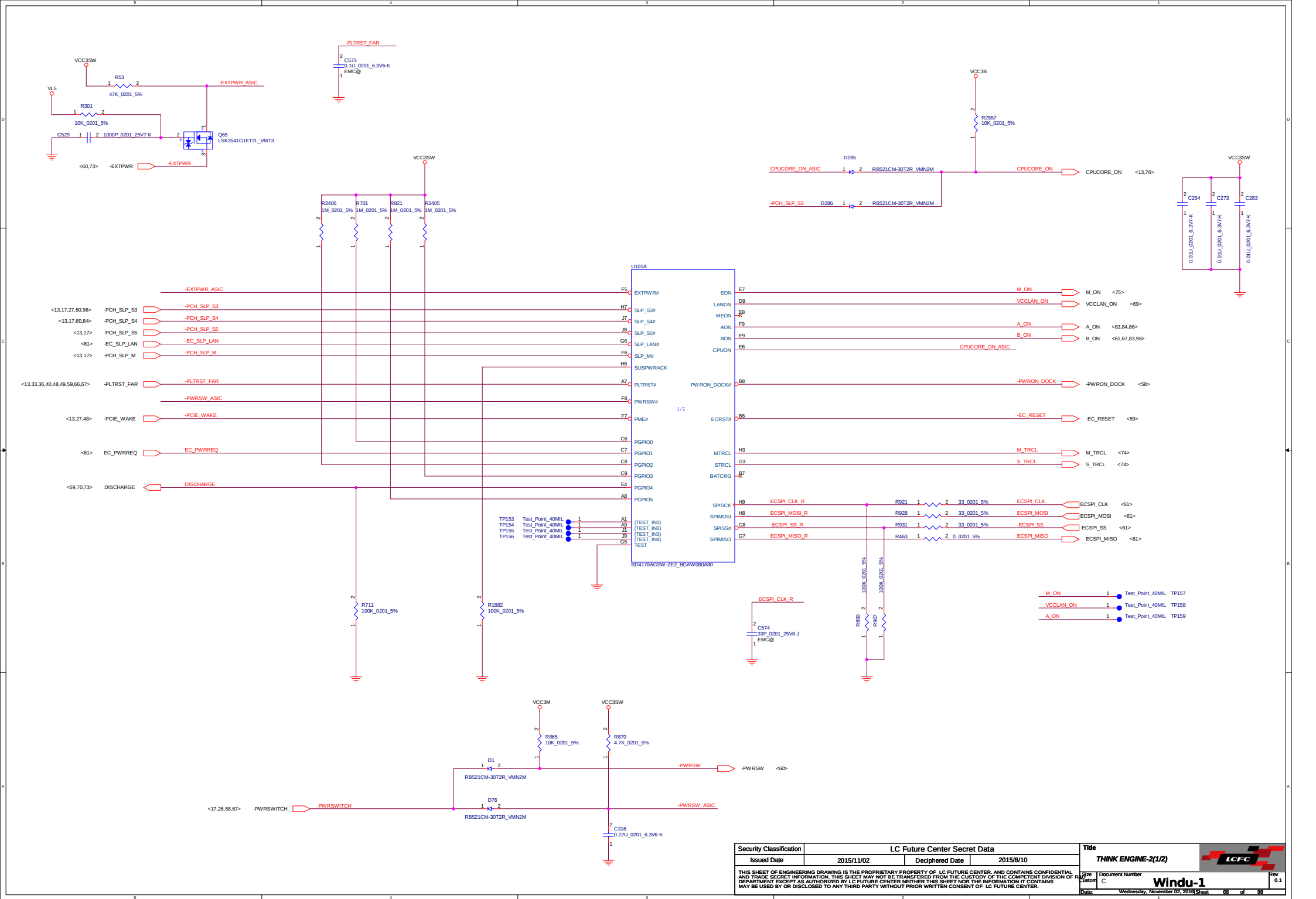


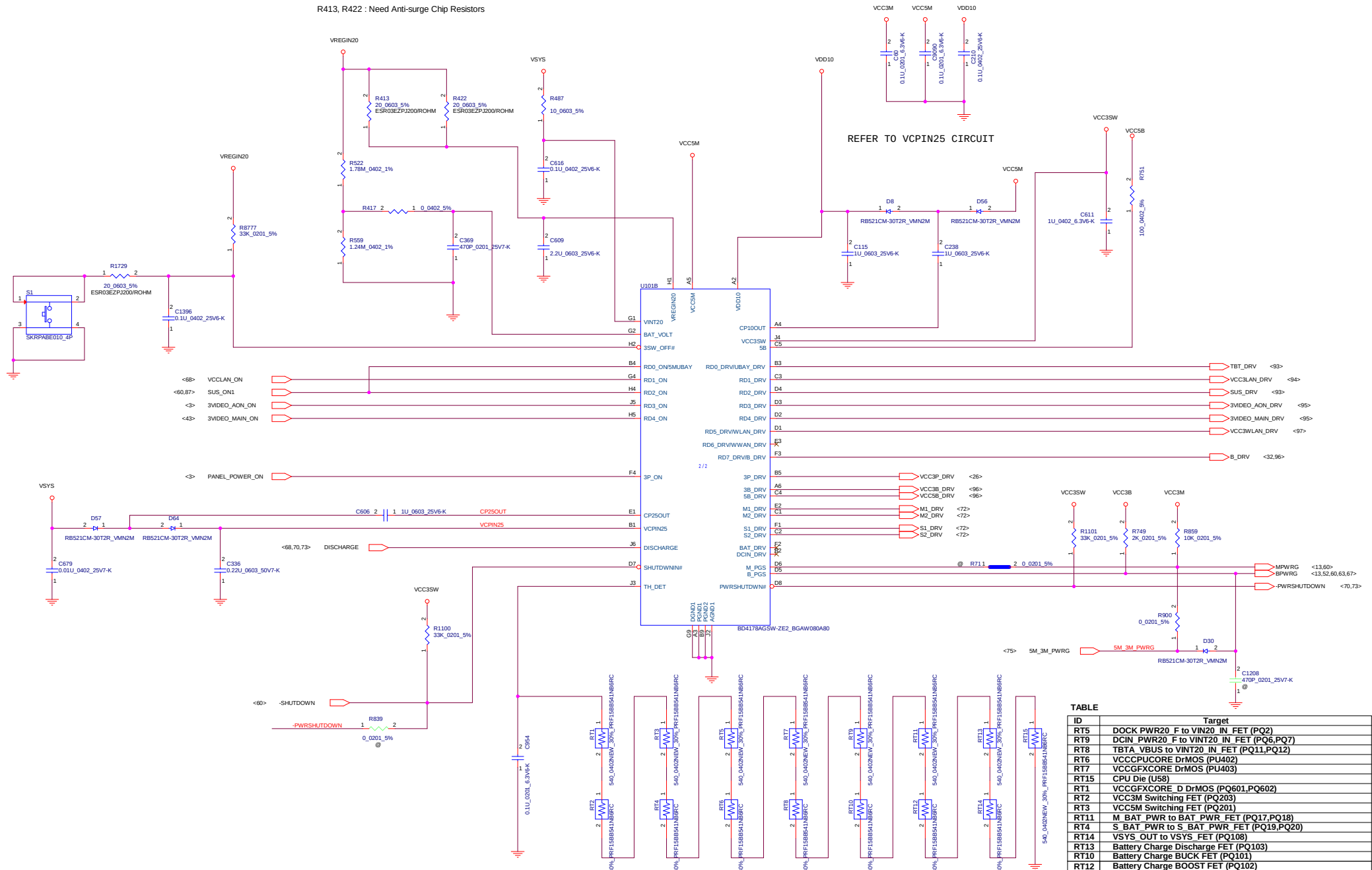
TABLE of U21/U31

Vendor	P/N	LCFC P/N
TOSHIBA	TC7SB385FU	SA00005US0J
ON	7SB385DFT2G	SA00007CW00






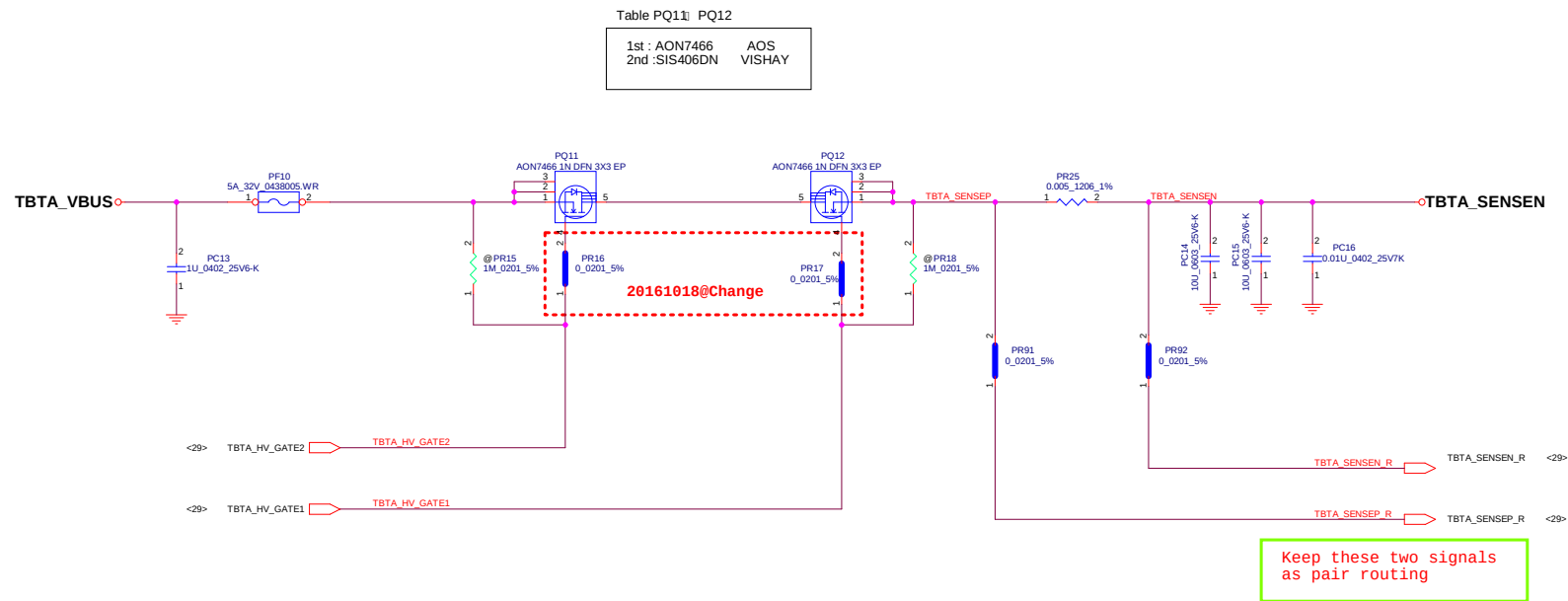
R413, R422 : Need Anti-surge Chip Resistors

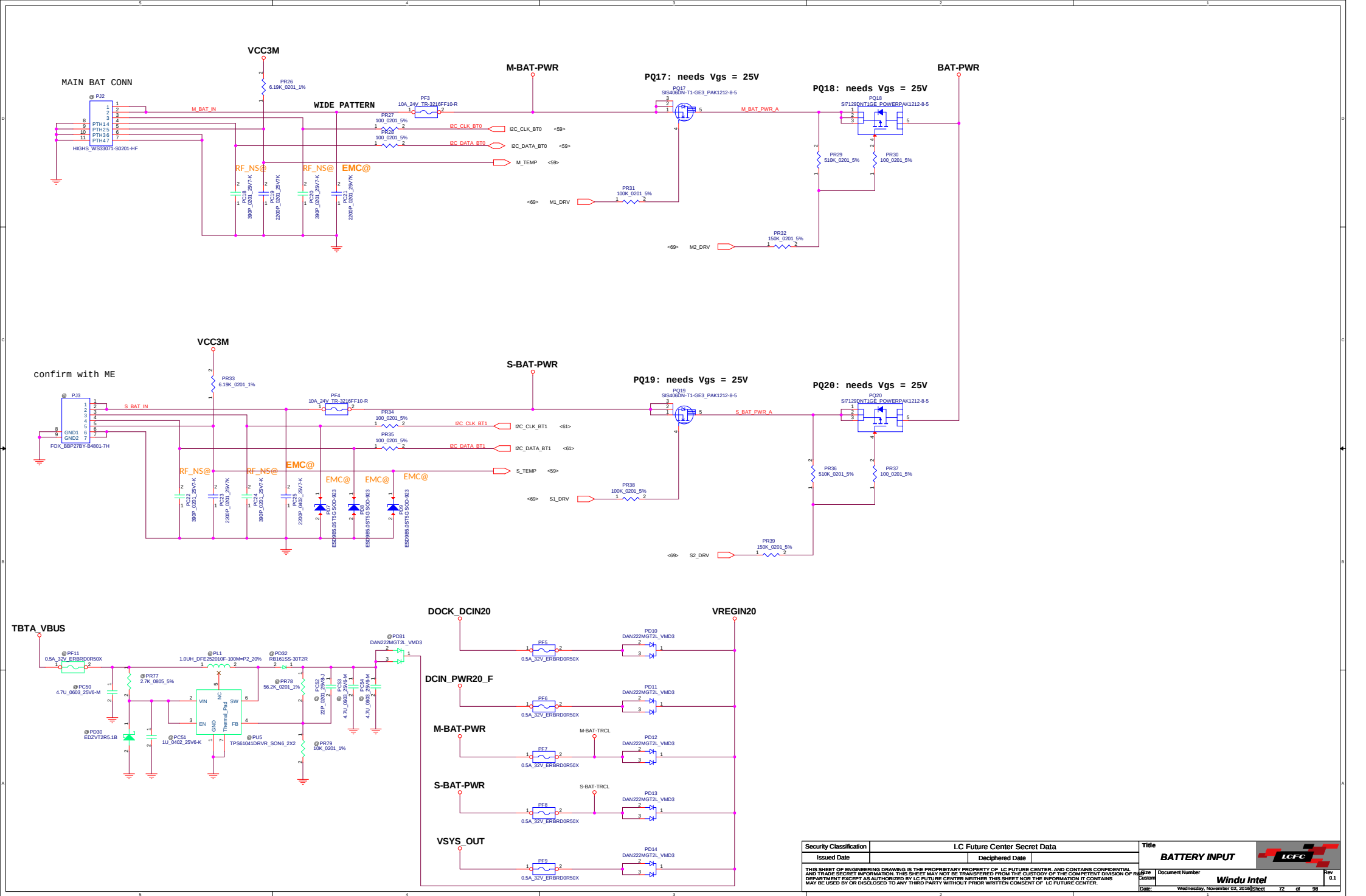


ID	Target
RT5	DOCK PWR20 F to VIN20 IN FET (PQ2)
RT9	DCIN PWR20 F to VINT20 IN FET (PQ6,PQ7)
RT8	TBTA VBUS to VINT20 IN FET (PQ11,PQ12)
RT6	VCCCPUCORE DmMOS (PU402)
RT7	VCCGFXCORE DmMOS (PU403)
RT15	CPU Die (U58)
RT1	VCCGFXCORE D MmMOS (PQ601,PQ602)
RT2	VCC3M Switching FET (PQ203)
RT3	VCC5M Switching FET (PQ201)
RT11	M BAT PWR to BAT PWR FET (PQ17,PQ18)
RT10	S BAT PWR to S BAT PWR FET (PQ19,PQ20)
RT14	VSYS_OUT to VSYS FET (PQ108)
RT13	Battery Charge Discharge FET (PQ103)
RT10	Battery Charge BUCK FET (PQ101)
RT12	Battery Charge BOOST FET (PQ102)

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/11/02	Deciphered Date	2015/08/10	THINK ENGINE-2(2/2)			
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Date: Wednesday, November 02, 2016 1:51				Window-1		69 of 98	







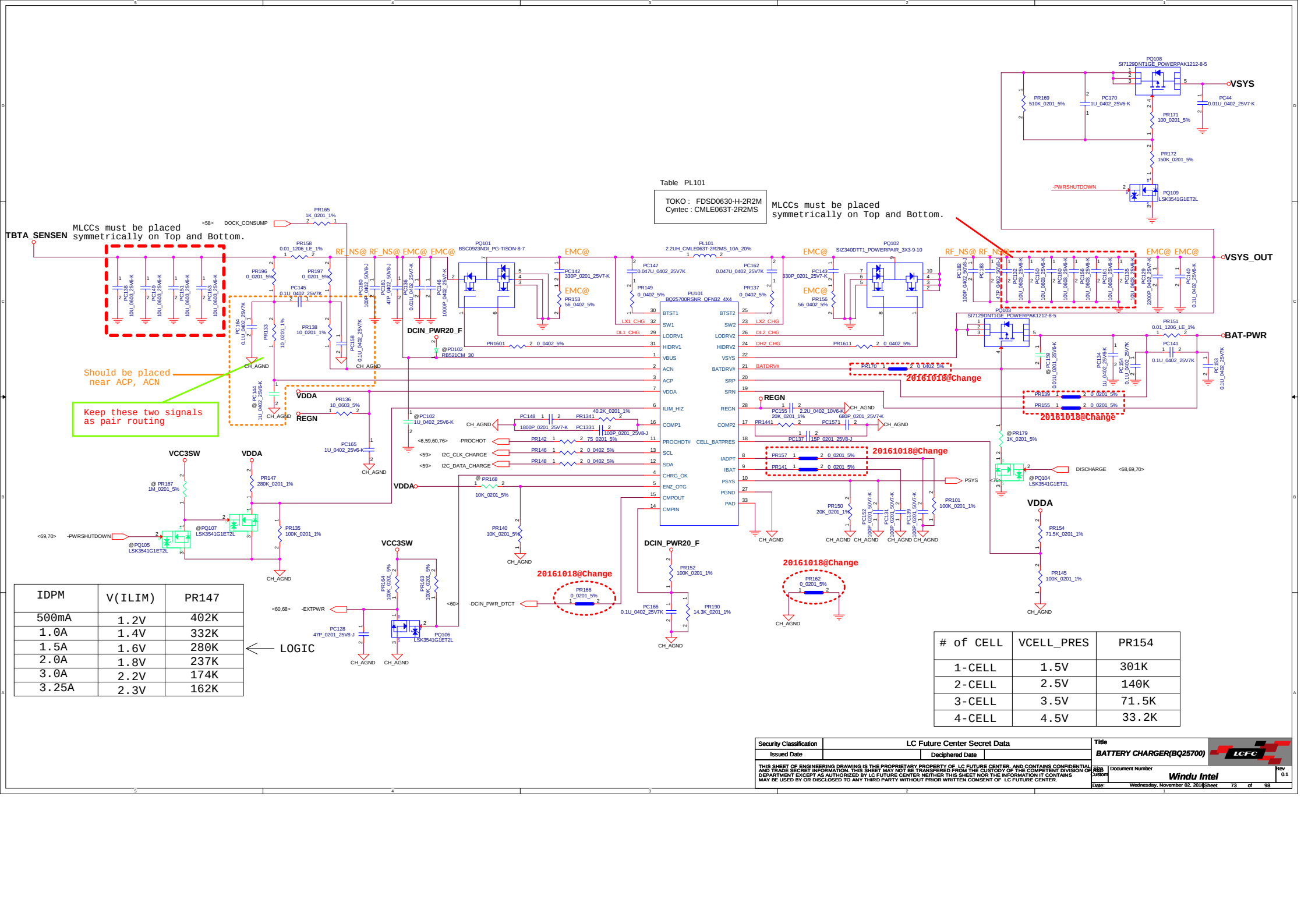


Table PL101

TOKO: FSD0630-H-2R2M  
Cyntec: CMLE063T-2R2MS

MLCCs must be placed symmetrically on Top and Bottom.

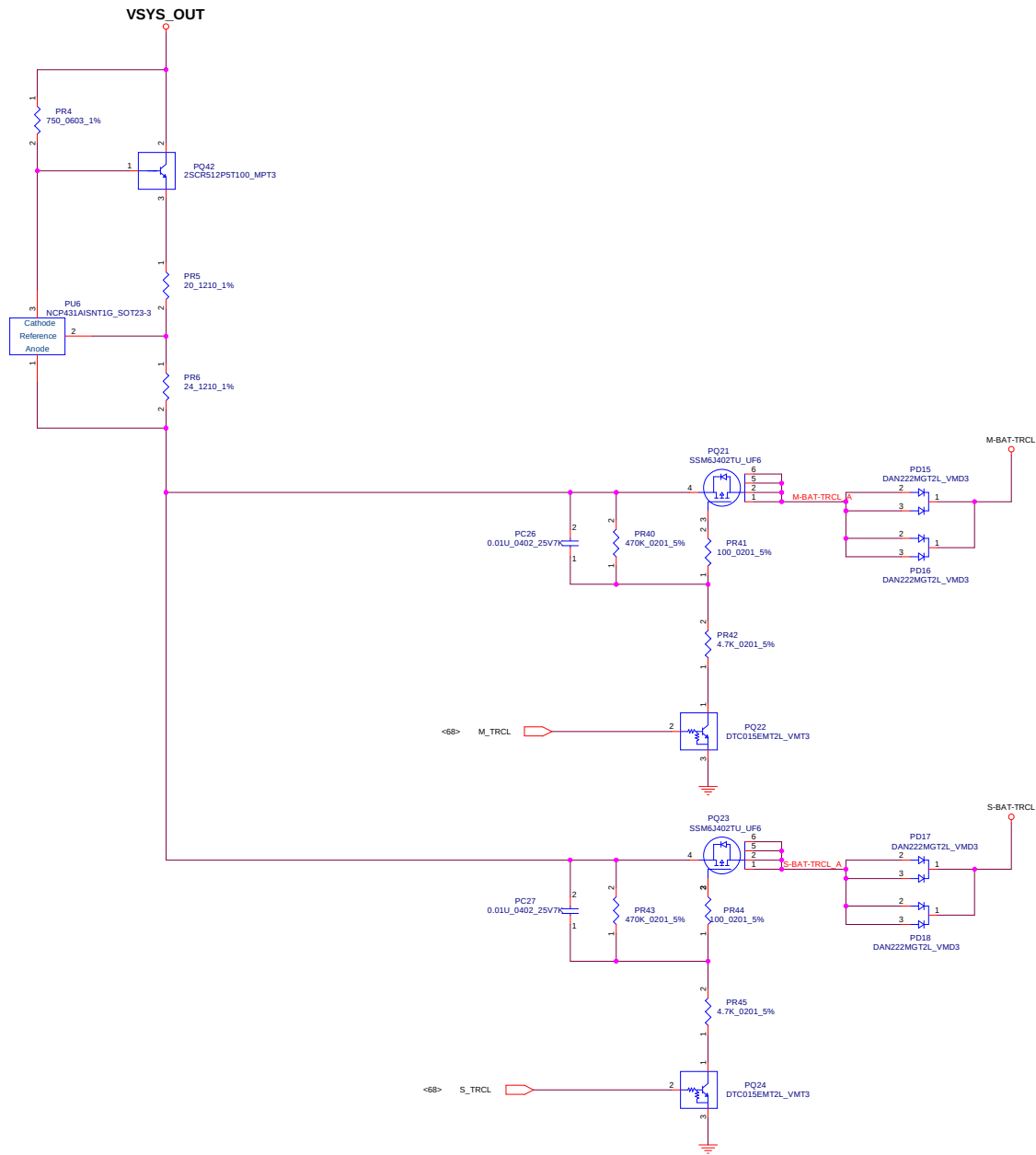
MLCCs must be placed symmetrically on Top and Bottom.

Should be placed near ACP, ACN  
Keep these two signals as pair routing

IDPM	V(ILIM)	PR147
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

LOGIC

# of CELL	VCELL_PRES	PR154
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K









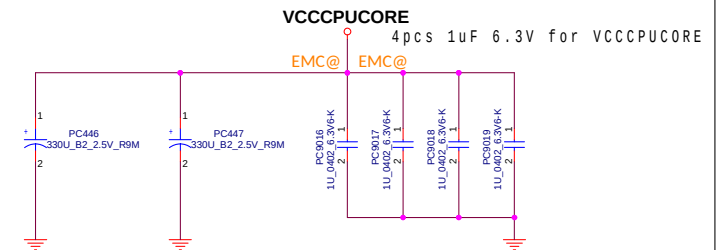
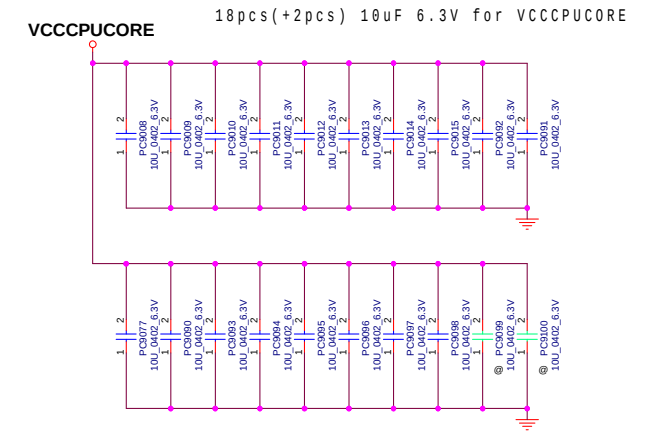
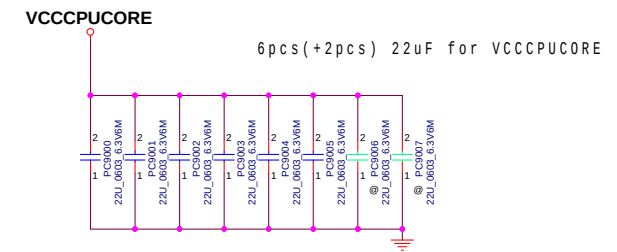
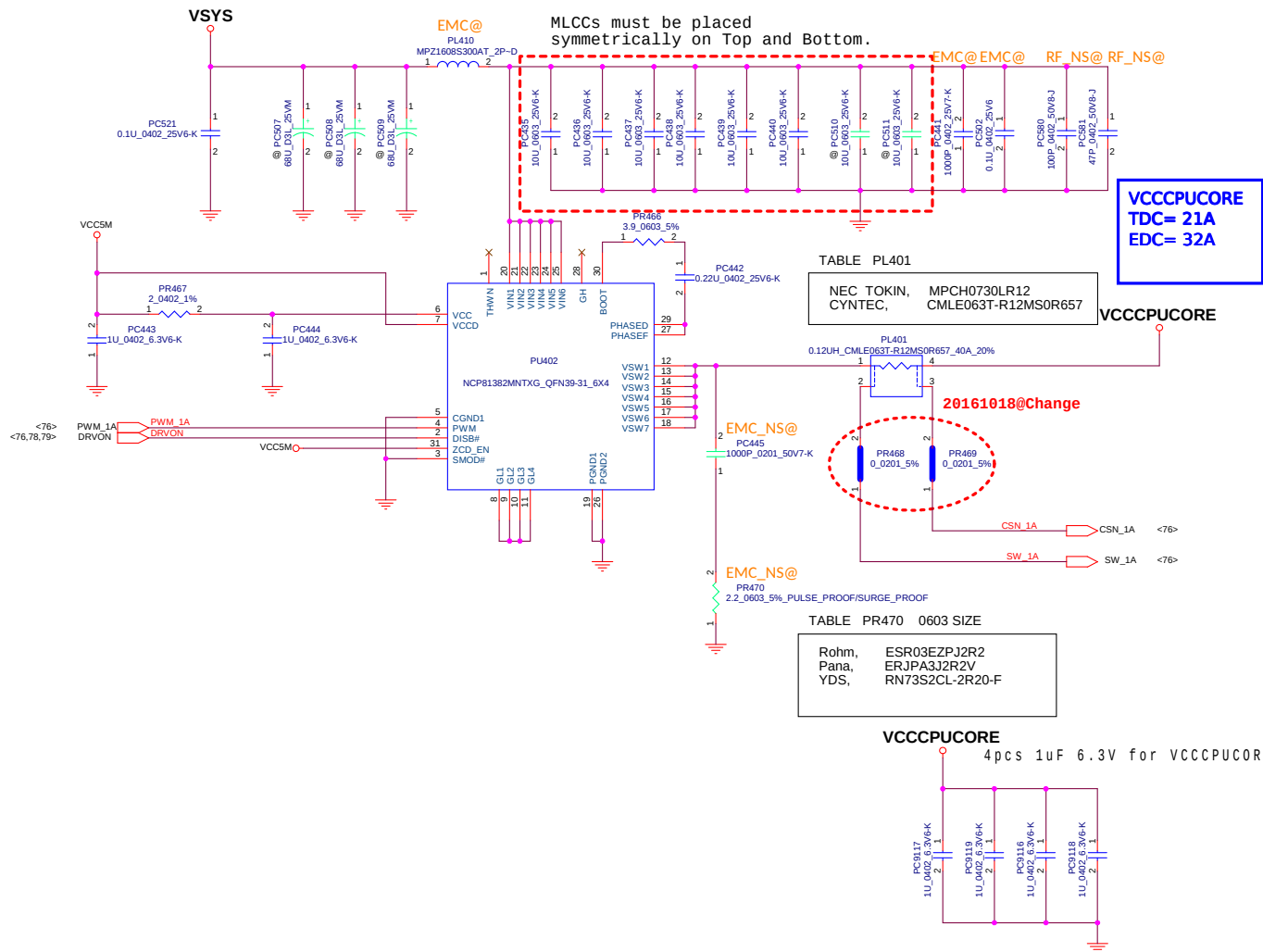
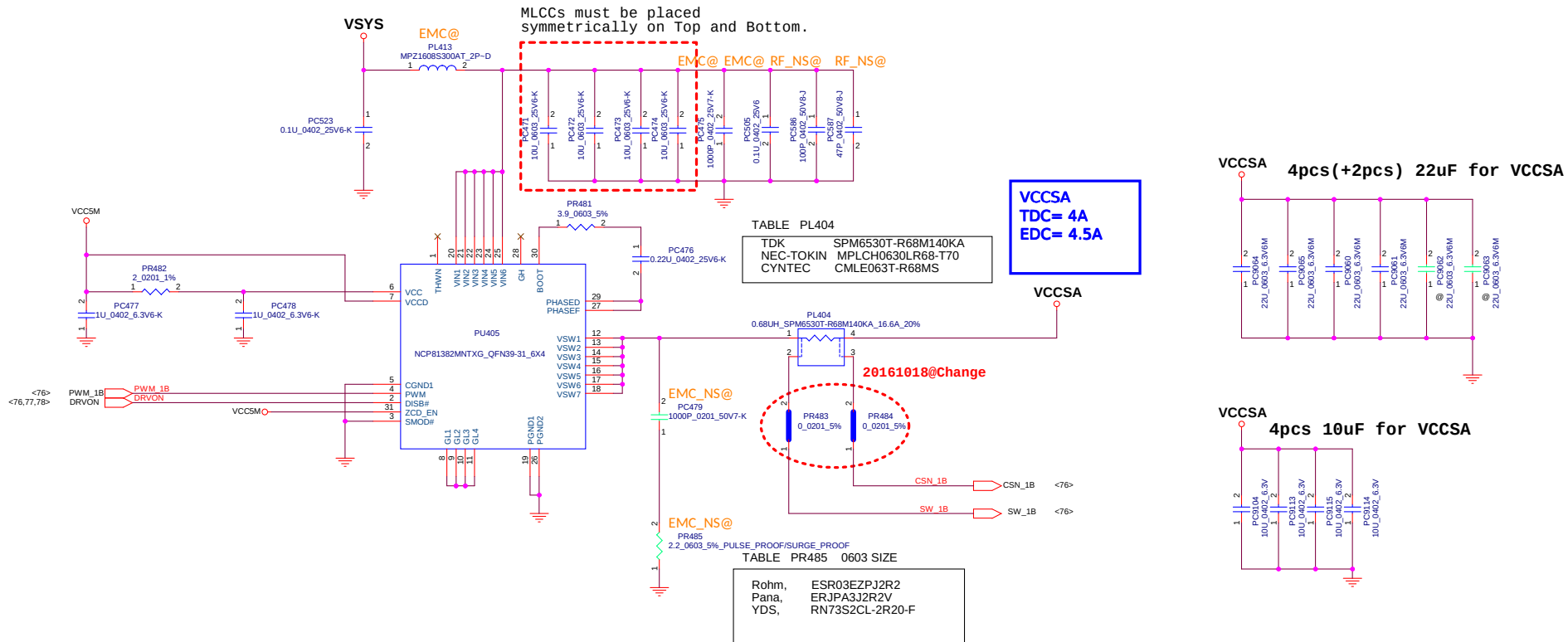



Table for PC446,PC447

Panasonic	ETPE330MA9L
NEC TOKIN	TEPSGB20E337M9-8R
KEMET	T520B337M2R5ATE009







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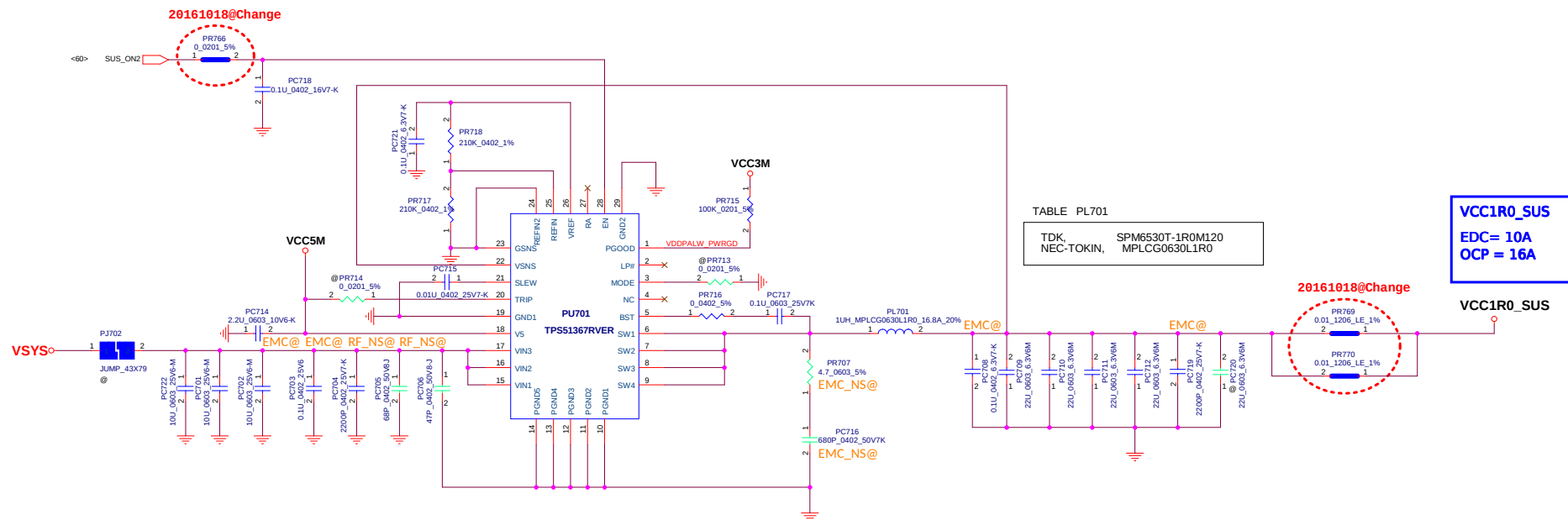
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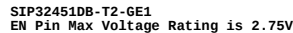
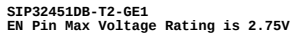
80 of 98


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				Custom					
								Date:	Wednesday, November 07, 2018



Mode	Frequency
GND	400KHz
Float	800KHz




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			Windu Intel Wednesday, November 02, 2011	Rev 0.1
			Sheet 83	of 98



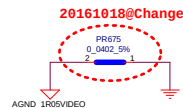


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LP#	C1	C0	VOUT
0	X	X	0V
1	0	0	0.8V
1	0	1	0.95V
1	1	0	1V
1	1	1	1.05V

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			Document Number	0.1
				
			Date: Wednesday, November 02, 2016 [Sheet 88 of 98]	

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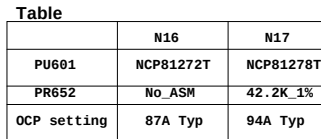
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Date: Wednesday, November 02, 2016					Sheet 90 of 98



Winda Intel

N16	N17
10K_1%	NO_ASM



**SWG\_EMC@ SWG\_EMC@**

MP2160BS300AT\_2P-D

oVSY

Table PL601

NEC-TOKIN : MPCH0730LR24  
TOKO : FDUE0630-H-R24M

SWG@  
PC606  
0.1U\_0402\_25V6-K

SWG@  
PC601  
S2090DT\_POWERARRRXS-8

7 PHASE1\_VGA

0.24U\_H\_MPCH0730LR24\_15A\_20%

SWG@  
PL601  
0.24U\_H\_MPCH0730LR24\_15A\_20%

SWG\_EMC\_NS@  
PC608  
470P\_0201\_50V7-K

SWG\_EMC\_NS@  
PR604  
2.2\_0603\_5%\_PULSE\_PROOF/SURGE\_PROOF

Table: PC609 / PC610

MLCCs must be placed symmetrically on Top and Bottom.

1st: 2R5TPE470M7 PANASONIC  
2nd: T520V477M2R5TAE007 KEMET

SWG\_EMC@

MP2160BS300AT\_2P-D

oVSY

Table PL602

NEC-TOKIN : MPCH0730LR24  
TOKO : FDUE0630-H-R24M

SWG@  
PC657  
0.1U\_0402\_25V6-K

SWG@  
PC602  
S2090DT\_POWERARRRXS-8

7 PHASE2\_VGA

0.24U\_H\_MPCH0730LR24\_15A\_20%

SWG@  
PL602  
0.24U\_H\_MPCH0730LR24\_15A\_20%

SWG\_EMC\_NS@  
PC631  
470P\_0201\_50V7-K

SWG\_EMC\_NS@  
PR624  
2.2\_0603\_5%\_PULSE\_PROOF/SURGE\_PROOF


SWG\_EMC@

VCCGFXCORE\_D

VCCGFXCORE\_P

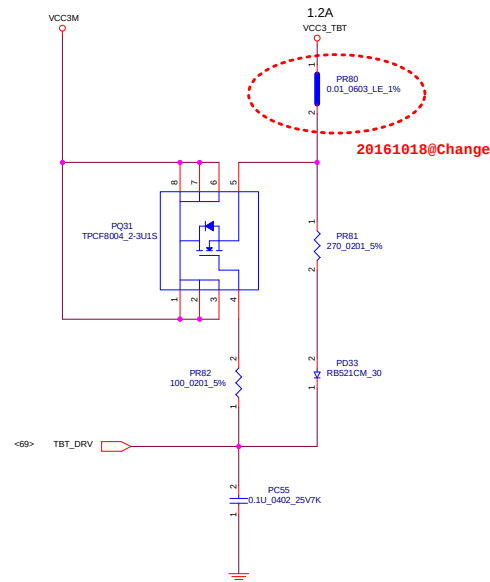
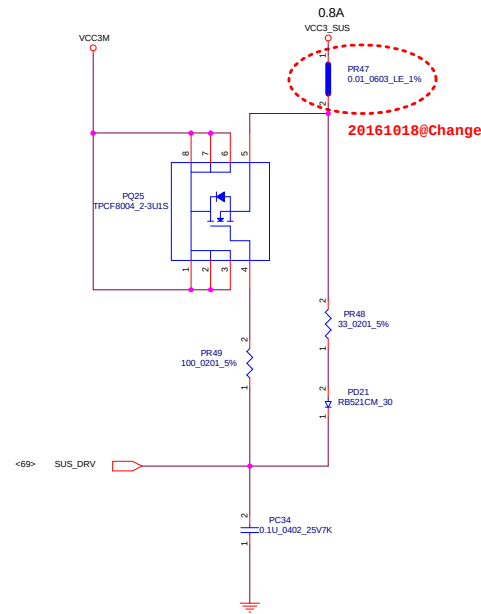
VCCGFXCORE\_D  
TDC = 28A  
EDC = 53A  
OCP = 87A

MLCCs must be placed symmetrically on Top and Bottom.

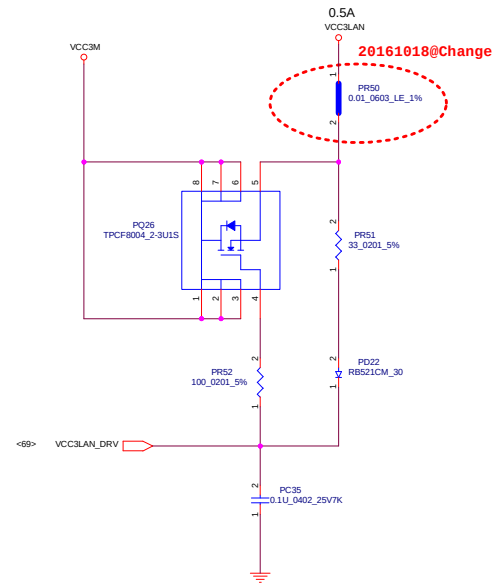
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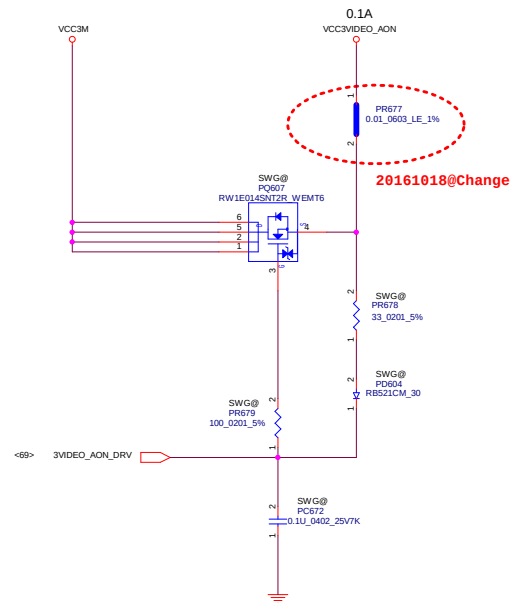
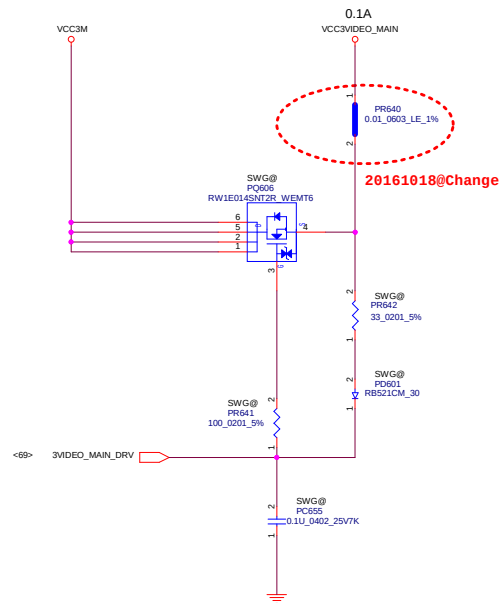
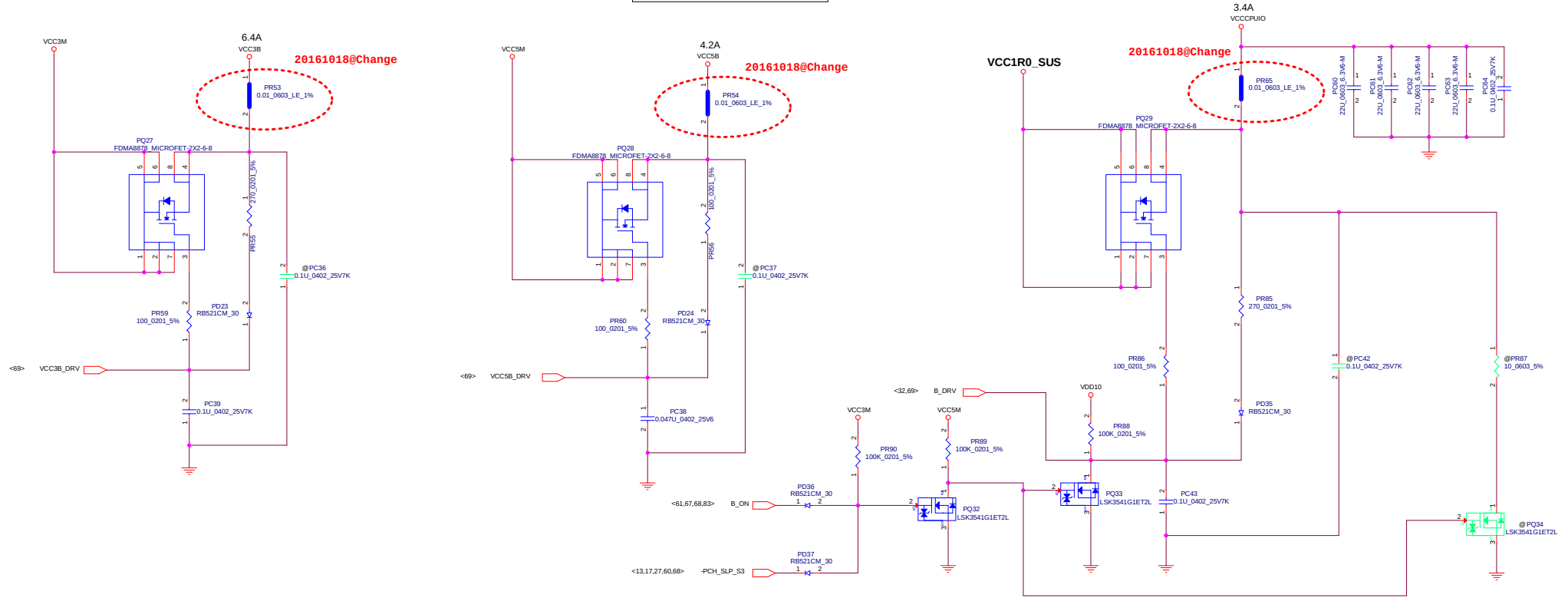
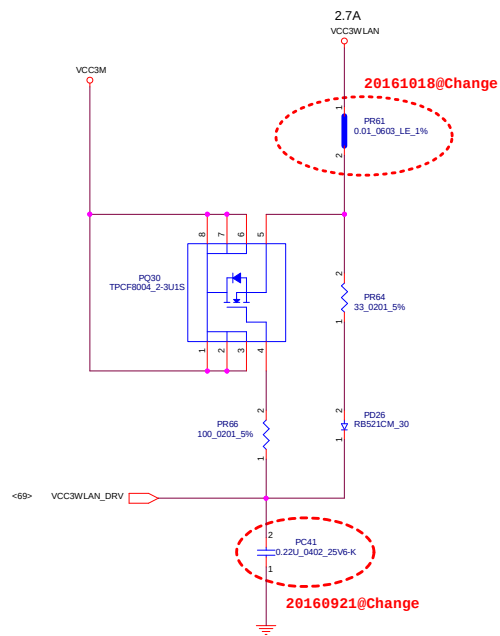


Table for PQ27: PQ28: PQ29

FAIRCHILD FDMA8878  
VISHAY SIA462DJ





TABLE

A0AC	YES	NO
PR70	NO - ASM	ASM
PQ35	ASM	NO - ASM
PR72	ASM	NO - ASM
PR74	ASM	NO - ASM
PC40	ASM	NO - ASM
PD23	ASM	NO - ASM

↑  
LOGIC

